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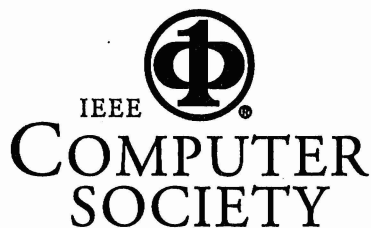
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2D Silicon/Ferroelectric Liquid Crystal Spatial Light Modulators

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David Banas, Stephen D. Gaalema, David J. Ward**

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2D Silicon/Ferroelectric Liquid Crystal Spatial Light Modulators

We have developed a spatial light modulator technology based on foundry silicon fabrication processes. This technology employs a thin, ferroelectric liquid crystal light-modulating layer at the substrate's surface, producing electrically addressed display devices with resolutions up to 256×256 and frame rates up to 10 kHz. We have also fabricated optically addressed smart-pixel arrays for low-level image processing. Performance has advanced rapidly due to design innovations and effective use of modern process features.

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Spatial light modulator (SLM) technologies have received fresh interest with the widening of applications for optical signal processing and the rising demand for small-format displays. Wide recognition of the versatility of silicon as an electronic material and the wealth of knowledge available on it has motivated researchers to devise SLM technologies that combine silicon with various light-modulating materials and devices.¹

Investment in time and money for silicon fabrication is enormous, making commodity silicon a bargain that is hard to beat. Using standard processes is so inexpensive compared to the alternative that it is worth adapting a design approach to the nature of this resource. Our challenge is to accommodate those characteristics of foundry VLSI that are at odds with the requirements of good SLMs.

We use standard or nearly standard commodity CMOS fabrication services provided by silicon foundries to produce chips that realize all but the light-modulating function of electrically or optically addressed SLMs. Post-processing steps can then incorporate a light-modulating layer onto the chips to turn them into complete SLMs.

The properties of the light-modulating material incorporated with the VLSI determine the use-

fulness and practicability of the resulting SLM technology. Ferroelectric liquid crystals (FLCs) with switching speeds at or below 100 μ s operate 100 times faster than the twisted-nematic materials used in early liquid crystal light valves. Further, their mechanical properties are convenient. Being isotropic liquids at convenient temperatures (around 100°C), FLCs are compatible with straightforward procedures for creating and filling thin cells.

Ferroelectric liquid crystals and SLMs

Figure 1 (next page) shows how we incorporate a light-modulating layer on the surface of a chip. Cells are specified at chip design time by laying out cuts in the passivation glass above metal pads. The pads serve both as mirrors and switching electrodes. A window carrying a transparent conductive layer, usually indium-tin oxide (ITO), and a rubbed polymer molecular alignment layer, is contacted directly to the chip surface. The window forms the top bounding surface of the cells and provides a common reference electrode. Attaching the window and filling the chips with FLC material are the only steps performed to turn them into SLMs.

The thinness of the cells (1 to 2 μ m) causes the FLC molecules to align in the surface-stabilized configuration.² In this mode, the FLC layer

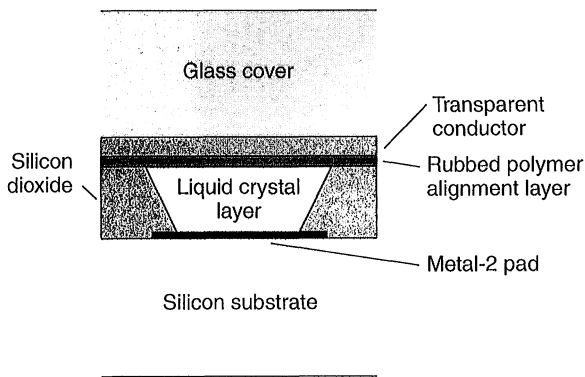


Figure 1. Typical silicon/FLC light modulator cell cross section.

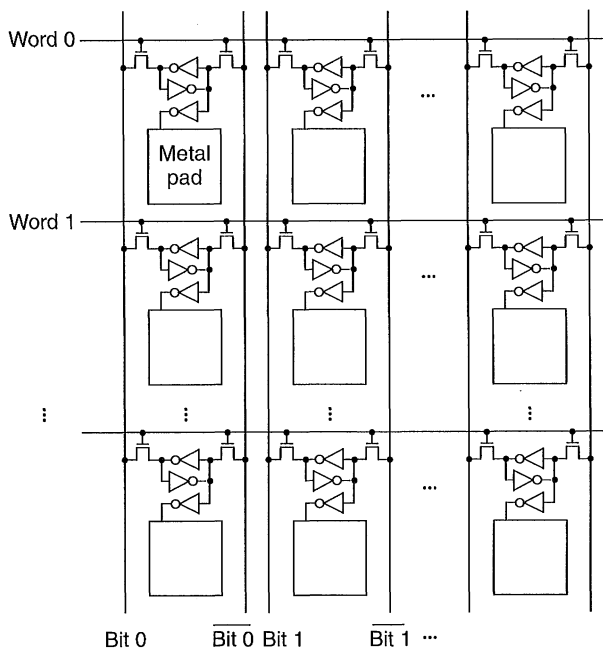


Figure 2. Pixel array circuitry of SRAM-based 64x64 SLM.

behaves optically as a uniaxially anisotropic slab with its slow axis in the plane of the bounding surfaces. When the electric field reverses, the slow axis rotates through 45 degrees. Suitable configuration of the input polarization yields a 90 degree modulation of polarization rotation, which gives rise to amplitude modulation between crossed polarizers. Electric fields of $2.5V/\mu m$ effect switching of the newer materials in 50 to 100 μs . Such fields are easily generated on a CMOS VLSI chip, and the circuit loading of a $50\text{-}\mu m \times 50\text{-}\mu m$

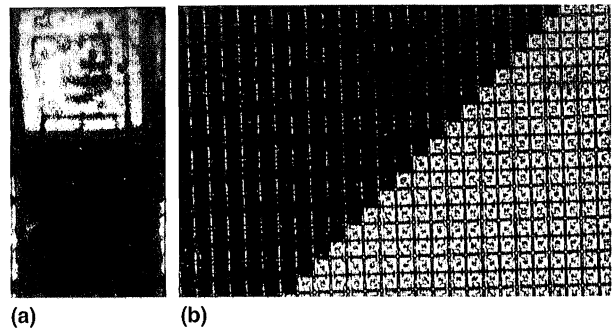


Figure 3. Photographs of a few cells of the 64x64 SRAM SLM (a), and most of the array (b), with an image displayed.

FLC cell is comparable to that of a few minimum-geometry logic gate inputs. This match in drive requirements makes silicon and FLCs a natural technology combination.

Three generations of electrically addressed SLMs

We have constructed electrically addressed SLMs by augmenting conventional static or dynamic random-access memory (SRAM or DRAM) designs with FLC light modulators. Our devices associate one modulator with each RAM cell; the binary-valued cell state drives the modulator. Interfacing to these devices is straightforward because, electrically, they resemble standard RAM parts. The designs we describe next appeared at approximately equal intervals over a five-year period. Their descriptions should convey a sense of the evolutionary pace of this SLM technology, how its progress has been tied to advances in silicon technology, and future improvements to anticipate.

64x64 SRAM-based SLM with 60- μm cell pitch. Our first device was fabricated in a $3\text{-}\mu m$, double-metal process, based on SRAM cells of the form shown in Figure 2. The cross-coupled static inverters, coupled by nMOS pass transistors to a pair of Bit lines, constitute a standard, six-transistor, static design. An additional inverter buffers the stored state and drives a second-metal pad that completely covers the cell. This switching electrode is driven to 0V or 5V. With the common window electrode held at 2.5V, the two possible cell states result from generating equal but opposite electric fields across the FLC. We chose an 8-bit-wide data input for easy interfacing to a PC provided with a plug-in interface card. Thus, each row of the 64×64 array fills in eight write cycles.

Choosing a static cell design eliminated the need for complex drive circuitry with critical timing specifications, and thus eased the verification and demonstration of this first device. Also, the additional buffer in each cell assures that the electrical state of the memory cell is isolated from that of the

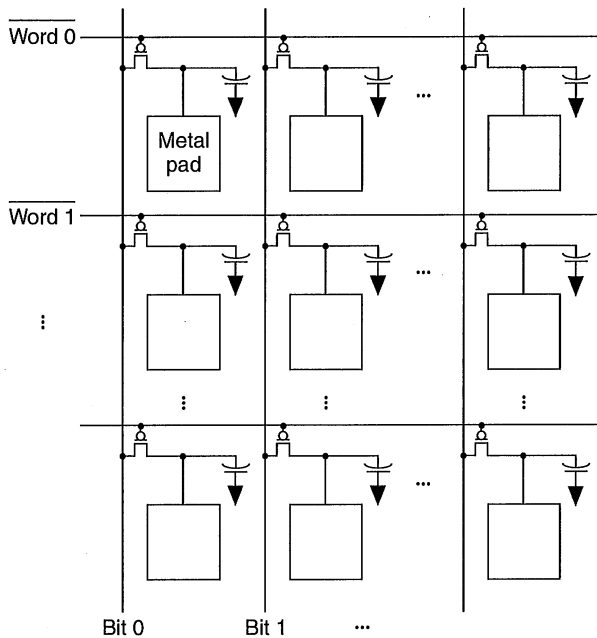


Figure 4. Pixel array circuitry of DRAM-based 256×256 SLMs. Each cell comprises a single-pass transistor controlled by a Word line, which gates the cell's internal capacitance onto a Bit line.

FLC. This means that a group of eight cells can be selected, written, and deselected in just nanoseconds, and writing a new group can begin while the first group is still switching. In fact, the entire array can be written in much less than the approximately 100- μ s FLC cell switching time.

Photographs of a few cells and of the whole array with a displayed image appear in Figure 3. Cells are on a 60- μ m pitch. The texture visible within the bright cells results from thickness variations in the FLC film. Variations occur because of the undulating topography of the circuitry beneath the second-metal layer. The fabrication process' 5- μ m second-metal spacing rule and the provision for individual passivation cuts for each cell determined the 67-percent area fill factor. We measured intensity contrast ratios of 12:1 using 633-nm HeNe laser light. The SLM operated at a 4.5-kHz frame rate without attenuation of the peak-to-peak optical response.³

256×256 DRAM-based SLM with 20- μ m cell pitch. The static cell design has advantages, such as easily met drive requirements and drive pipelining, but requires too much area for use in high-resolution displays. We implemented our next design in a 2- μ m process and also moved to a dynamic cell configuration, shown in Figure 4.

Since all the FLC switching charge must now come through

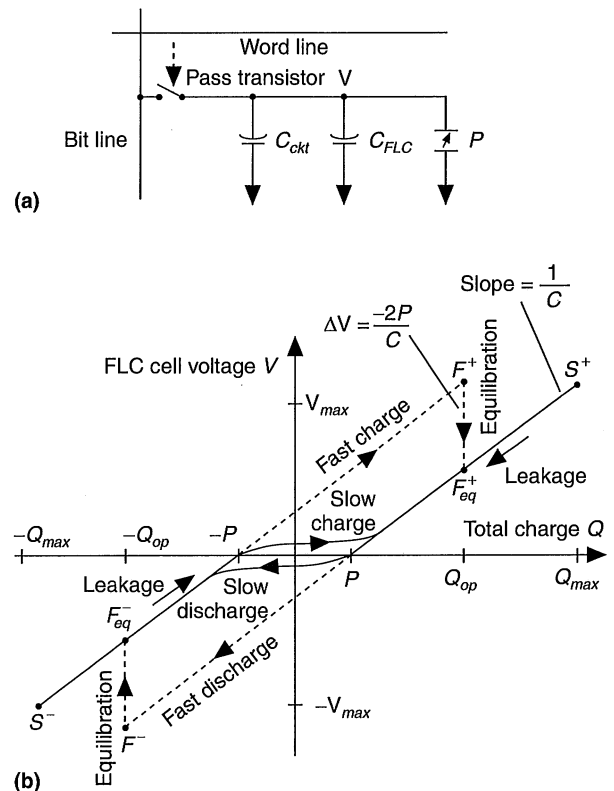


Figure 5. DRAM-style SLM pixel design: equivalent circuit (a) and voltage-charge characteristics (b).

the Bit line, charge dynamics within the cell become important, as does maximizing the time the cells connect with their Bit lines. To accomplish the latter, we incorporated a 256-bit-wide pipeline register into the data path. To write a row, 32-bit words are read sequentially into eight registers. These word registers then dump in parallel into the full-row pipeline register. The register's contents are gated onto the Bit lines, while the word registers are loaded with the next row's data. Thus, each cell is driven by its Bit line during the active phase of a Word line cycle that lasts practically 1/256th of the frame time. At television frame rates, the resulting 65- μ s Word cycle is commensurate with the FLC switching time. However, framing at 4 kHz reduces this time to less than 1 μ s. How does this affect the writing process?

Charge dynamics of the FLC now come into play. Physically, we can model the modulator cell as a suspension of electric dipoles in a viscous dielectric fluid, bounded by parallel-plate electrodes. Figure 5a shows the pass transistor as a switch, and C_{ckt} represents the combination of an explicit MOS capacitor with other parasitic circuit capacitances. We represent the FLC cell as the parallel combination of linear

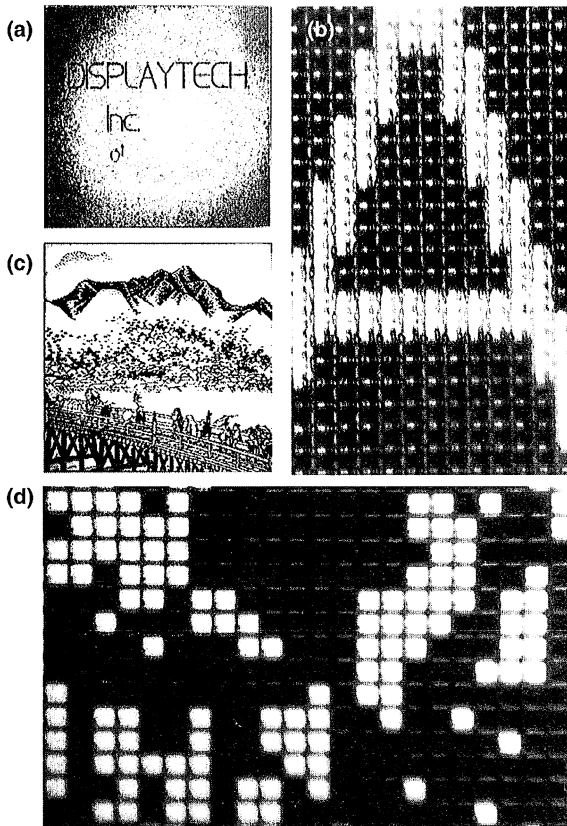


Figure 6. Photographs of images displayed on 256x256 Generation-2 SLMs: entire array (a) and a few cells (b). Similar images from a Generation-3 SLM: entire array (c) and a few cells (d).

capacitance C_{FLC} with a field-controlled dipole distribution having spontaneous polarization P .

Spontaneous ferroelectric polarization p_s of these materials is between 30 and 40 nC/cm². Under DC bias, all dipoles align with the electric field. When the field reverses, the dipoles follow, hindered by viscosity. To reverse all dipoles in a cell of area A , a charge of

$$Q_{sw} = 2P = 2Ap_s$$

must pass between the electrodes, where P denotes the cell's total spontaneous polarization charge. This charge movement takes place over the FLC switching time τ , approximately equal to 100 μ s.

Figure 5b is a plot of cell voltage V versus the total charge Q stored in the pixel circuit under the simplifying assumption that $C = C_{FLC} + C_{cbt}$ is linear. The slope of the asymptotes

is $1/C$, and they intercept the charge axis at $\pm P$. The solid line shows state evolution for very slow modulation of V between $-V_{max}$ and V_{max} . Dashed lines represent fast SLM operation.

When V changes slowly over a time that is large compared to τ , the plot traverses the solid path shown. When $|Q| < P$, an additional charge increment causes dipoles to flip and does not substantially affect voltage. When $|Q|$ exceeds P , dipoles are all aligned with the applied field, and a charge increment is stored on the linear capacitance C , with a concomitant change in voltage. Charging the circuit slowly to V_{max} (or $-V_{max}$) leaves it in the state labeled S^+ (or S^-).

Now suppose the cell is in state S^- , is charged rapidly to V_{max} , and then isolated from its Bit line. There is no time during charging for dipoles to flip, so the cell behaves like a linear capacitor and follows the "fast-charge" path to F^+ , in which state a total charge of Q_{cp} is stored. Isolated from its Bit line, the cell now seeks equilibrium as its dipoles begin to flip. Since charge is conserved, the cell's state follows the vertical equilibration path to state F^+_{cp} , and the cell voltage drops by $2P/C$. However, as long as $Q_{cp} > P$, the cell equilibrates to a fully switched state. A certain margin is desirable to compensate for charge leakages that occur between refreshes. A reasonable figure of merit for the electrical cell design is

$$Q_{cp}/P = [V_{max}(C/P)] - 1 = [V_{max}(C_{cbt} + C_{FLC})/P] - 1$$

which should be made greater than unity. For a given FLC material and chosen operating wavelength, C_{FLC}/P is constant. V_{max} is typically limited to half the supply voltage, so the key to a robust, fast DRAM SLM design is providing adequate "ballast" capacitance in the cell.

The Generation-2 SLM employs an explicit MOS capacitor that occupies the 16 percent of the pixel area available for it, and contributes about 50 fF to the cell capacitance. This is sufficient to switch FLC materials with polarizations up to at least 30 nC/cm². We also improved fill factor over the Generation-1 device to 72 percent, despite a reduction in pixel pitch. Exploiting the tighter metal-2 design rule and eliminating individual passivation openings above the modulator pads in favor of a common, large cut accomplishes this.

A sophisticated interface drives the SLM. Part of it resides on a PC-compatible plug-in card, and the remainder fits within the mounting fixture for the device. FLC materials, like all liquid crystals, are susceptible to degradation from sustained DC electric fields. Although refinement of these materials to extreme purity levels has increased their tolerance of the mechanisms involved, it is still important to render the average voltage applied to each cell as close to zero as possible. The driver circuitry does this automatically by alternately displaying asserted and inverted versions of each input image. Strobing the incident illumination to coincide with only the asserted phase of each image prevents the displayed image from washing out. This strategy halves the usable frame rate

but does not reduce optical throughput.

Full-aperture and close-up photographs of an image written to the Generation-2 SLM appear in Figures 6a and 6b. The pixels appear much more uniform than those of the SRAM device, and contrast improved to 29:1 at a 4-kHz frame rate.⁴ Table 1 summarizes the Generation-2 SLM's electrical and optical characteristics, and introduces two important performance criteria: optical throughput and illumination tolerance.

Optical throughput is the efficiency with which the SLM transforms incident light into a usable output image. Area fill factor of the modulator electrodes is important because incident light falling between these reflectors is lost and counts against throughput. However, for information-processing applications, other factors play a role. The pixelated nature of the SLM means that fundamentally, it displays a sampled version of a desired image. Sampling an image manifests in the frequency domain as a replication of the original image's spectrum. Physically, these replicas propagate in different directions away from the device, and it is practical to use only one of them—usually the zero-order (on-axis) copy—in a coherent image-processing system.

The optical structure of individual pixels is important because, according to sampling theory, the Fourier transform of the light from a single "on" pixel constitutes a multiplicative envelope for the entire spectrum. An optically smooth pixel gives rise to an envelope concentrated at the origin and enhances the energy in the zeroth diffracted order. A highly textured pixel diffuses reflected-light energy into higher orders at the expense of the zeroth order. Thus the smoothness of the pixel mirror is as important as its area fill factor.

The second performance issue, illumination tolerance, relates both to area fill and to the previously discussed cell figure of merit Q_{off}/P . The source/drain implant regions of the cell's pass transistor form parasitic p-n junctions with the substrate. Even when the transistor is off, the inboard junction connects across the storage capacitor and FLC cell. This junction acts as a photodiode, and light illuminating the substrate causes cells to discharge. The more completely we cover the substrate with metal, the less light-sensitive the device becomes. For a given effective light responsivity of the parasitic photodiode, the time constant of discharge is proportional to illumination intensity and inversely proportional to the total cell capacitance. The illumination tolerance reported in Table 1 is the incident light intensity that makes a bright cell fade to half its initial output (over a period of four minimum refresh times) after isolation of the cell from its Bit line.⁴

The Generation-2 SLM demonstrated good speed performance and reasonable contrast. However, it possessed poor optical throughput and only marginal tolerance to bright illumination. As we see later, increases in area fill factor, cell smoothness, and cell capacitance alleviate these shortcomings.

256×256 DRAM-based SLM with 30- μ m cell pitch. The Generation-3 design shows how effective use of silicon

Table 1. Characteristics of 256×256 DRAM SLMs.

Type	Characteristic	Generation	
		2	3
Geometric	Aperture (mm ²)	5.12	7.68
	Design rule (μ m)	2	1.2
	Pixel pitch (μ m)	20	30
	Mirror gaps (μ m)	3	1.6
	Mirror area fill factor (percent)	72	90
Electrical	Data-bus width (bits)	32	32
	Nominal data clock (MHz)	20	80
	Row address time (ns)	460	100
	Frame update time (μ s)	118	25.6
Optical	Optical rise/fall time (μ s)	225	105
	Frame rate (kHz)	4	10
	Image contrast ratio	29:1	100:1
	Throughput into zero order (percent)	< 1	10
	Illumination tolerance (mW/cm ²)	20	>10,000

process refinements can lead to large performance gains. We did not change the circuit design in this device qualitatively, but reengineered it to support a total information throughput of 2.6 Gbps.⁴ Two significant changes were moving to a 1.2- μ m CMOS fabrication process and increasing pixel pitch to 30 μ m. Full-aperture and close-up photographs of an image written to the Generation-3 SLM appear in Figures 6c and 6d. Reengineering dramatically improved contrast and pixel homogeneity. Table 1 summarizes Generation-3 SLM characteristics and reveals additional improvements; we account for these as follows.

In the finer-line process, we could make the cell pass transistor smaller. Straightforward scaling together with the larger pixel pitch left 62 percent of the pixel area for the MOS capacitor, up from 16 percent. The reduction of gate oxide thickness in the 1.2- μ m process also increased the specific MOS capacitance by a factor of 1.8, to 1.5 fF/ μ m². The combined effect of these changes was to increase cell capacitance to nearly 1 pF. This change, together with an increase in fill factor to 90 percent, contributed to the realization of a 500-fold improvement in illumination tolerance.

The doubling of frame rate derives partly from using a faster FLC material and partly from a reduction in cell thickness to less than 1 μ m. The latter resulted from improved fabrication techniques.

Throughput into the zeroth diffracted order also improved dramatically (to 10 percent), thanks to three factors. First, the metal-2 fill factor is higher. Second, the topographically uniform MOS capacitor structure occupies a larger fraction of the

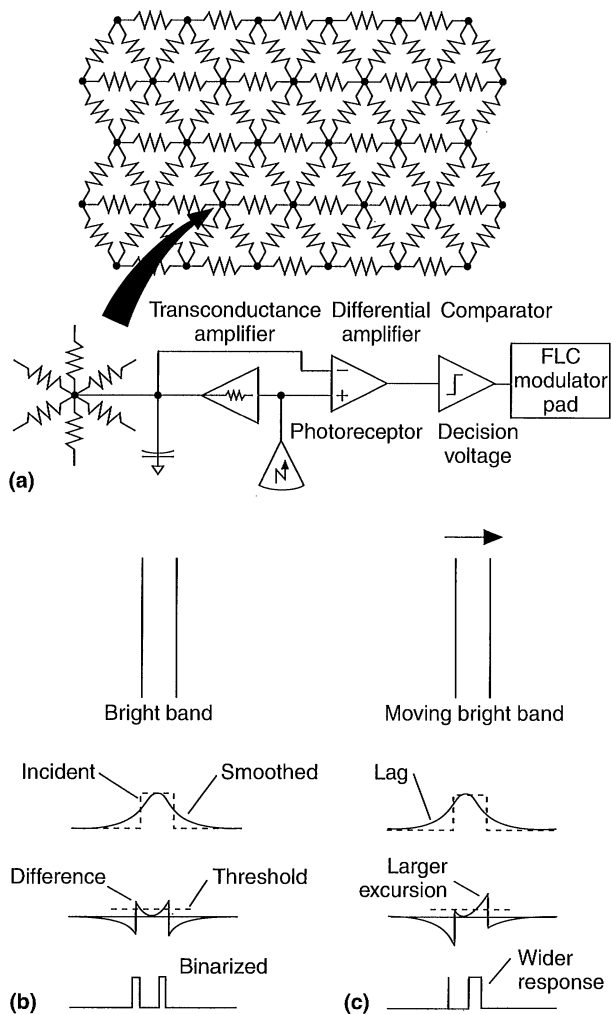


Figure 7. Mahowald-Mead silicon retina concept augmented with thresholding and optical output functions: focal plane circuit (a), response to a stationary bright band of illumination (b), and response to a moving band of illumination (c).

cell. Finally, the finer fabrication process is inherently more planar. VLSI process developers must themselves improve planarity as lateral geometries decrease. Electrical performance demands force metal and dielectric thicknesses to remain nearly constant. To avoid problems with the deposition of successive layers, process developers introduce explicit steps that smooth the wafer topography. Fabricating a given layout in the 1.2- μm process yields a smoother device than in the 2- μm

process. Contrast, improved to 100:1, also benefited from the flatter mirrors of the Generation-3 design.

The Generation-3 SLM characteristics cross the threshold into practical usefulness. However, the technology is young, and performance will progress much further before exhausting the potential of SLM fabrication refinements and modern VLSI processes.

Optical-in, optical-out smart focal plane devices

Edge detection and enhancement have long been important aspects of image preprocessing for pattern recognition and computer vision. Mahowald and Mead introduced a biologically inspired family of 2D, analog, VLSI focal plane structures that mimic aspects of the biological retina. They also exhibit edge detection, motion enhancement, and dynamic range compression.⁵ These devices employ parasitic bipolar devices as photodetectors to provide direct image input and convey their output image in serial electrical form.

As optical pattern recognition systems based on 2D correlation become more prevalent, demand rises for image preprocessing and low-level feature-extraction techniques that retain their outputs in optical form. We believe that smart, optically addressed SLMs in silicon VLSI/FLC technology are well matched to these tasks. We have therefore researched real-time edge- and motion-enhancing focal planes with optical image outputs.

Mahowald-style, edge-enhancing focal planes. Figure 7a reproduces the functional structure of the Mahowald retina in slightly augmented form. A hexagonal resistive net interconnects a 2D array of analog circuit cells. In each cell, a photoreceptor circuit exploiting the exponential sub-threshold current-voltage characteristic of diode-connected MOSFETs, generates an activation voltage. This voltage varies logarithmically with incident light intensity and drives a transconductance amplifier that tugs the net in the direction of its input. The net tends to diffuse away large spatial gradients to produce a smoothed version of the logarithmically compressed input scene. Capacitive loading causes temporal, as well as spatial, filtering. A difference amplifier that subtracts the smoothed signal from the incident signal generates each Mahowald cell's output. We have added the simple functionality of a comparator with programmable threshold driving an FLC modulator pad.

Figure 7b shows how the retina responds to a stationary bright band of illumination spanning multiple cells. The difference between the incident and smoothed activation profile is a bipolar, analog signal with peaks near contrast edges. The space constant of the device, evident in the decay profile of the peaks, depends on the ratio of the lateral conductance of the net to the amplifier transconductance. Placing the comparator threshold within the excursion range of the analog output generates a binary signal. In Figure 7b, the chosen threshold leads

to "on" pixels on the bright side of contrast edges. Sharper contrast steps generate wider bands of "on" pixels.

Figure 7c shows the retina's response to a moving bright band. The smoothed activation lags the incident signal because energy is stored on the net. The ratio of net capacitance to lateral conductance determines the time constant of this spatio-temporal filtering. Moving the illumination band enhances the analog output at the leading edge, and in turn produces a wider binary signal upon thresholding.

Thus the Mahowald retina detects edges and enhances motion. In a typical circuit realization, time and space constants are voltage tunable, which enhances the concept's flexibility. The thresholding and light modulation functions we have added turn the retina into a "magic mirror" that reflects only the interesting parts of an incident image.

A continuous-time retina design. We implemented a design of a 20x22 retina array in a 0.8- μm , triple-metal, CMOS process brokered through the MOS Implementation System. To address the challenge of preventing process parameter variations from corrupting intended circuit operation, we tested a photoreceptor circuit intended to reduce systematic input noise arising from global threshold variations. We used a dual-rail (differential) signal representation in conjunction with differential difference amplifiers for the gain elements. They fit naturally with the detectors' differential outputs and provided for easy programming of the comparator threshold.

The horizontal resistors of the hexagonal net are FETs biased into their linear region with Mead's HRES circuit. The open drains of the six FETs connect to mirror-image structures in neighboring cells. Resistors formed in this way are linear over a few tenths of a volt. The voltage programmability of the HRES circuit lets horizontal resistance vary over several orders of magnitude.

The improved density of the 0.8- μm process allowed us to pack the 48 devices of the cell circuit into a 72- μm x62.4- μm footprint. At this density, a 140x160 array would occupy 1 cm^2 . Figure 8 shows the surface topography of a few cells of the fabricated chip before light modulator assembly. We used the metal-3 layer exclusively for the reflective switching electrodes. The metal-3 gap rule is only 1.2 μm , but the provision of separate glass cuts above individual pads widened the dead space between pixels. The planarity of this process is so good that no hint of underlying circuit topography is visible in a photograph of the top layer.

Array layouts such as these—those having both a signal beam and readout (pump) light incident upon them—put three metal layers to good use. We must avoid leakage of the pump light onto the photodetectors, which would wash out the input image. In our design, interdigitated metal-2 power and ground buses occlude most of the area in the gaps between the metal-3 modulator pads. This greatly reduces capacitive coupling between the pads and the underlying circuitry. The resulting near-total occlusion of the sub-

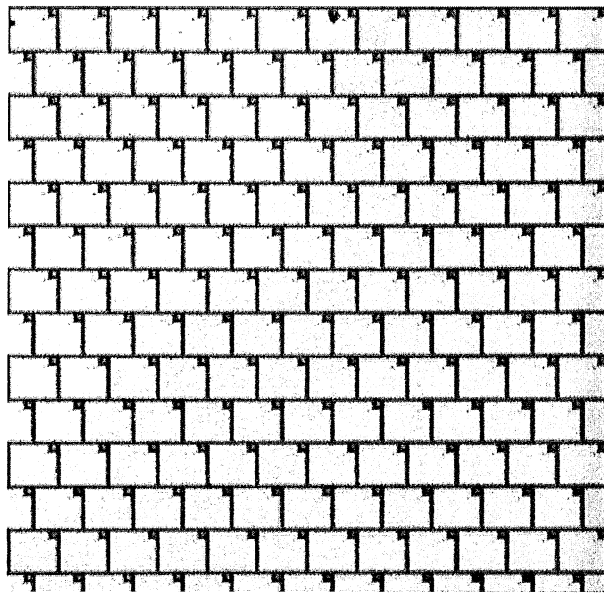


Figure 8. Photograph of a portion of the continuous-time retina cell array before FLC layer incorporation showing high fill factor and good flatness. The square notch cut from each rectangular modulating electrode exposes the phototransistor active region.

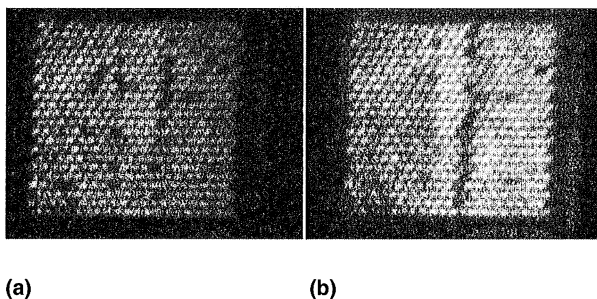


Figure 9. Photos of continuous-time retina output for a static dark bar (a) and dark bar moving to the left (b) showing motion enhancement.

strate between rows of phototransistors lets us format pump light into continuous parallel stripes. Imaging a Ronchi ruling mask (a transparency carrying opaque parallel stripes) onto the device accomplishes this easily.

Fundamentally, our retina is a 3-terminal device because an input data image controls the disposition of power from a separate supply (pump) beam into an output beam. Figure 9 shows two output frames of the device under excitation by a stationary and moving dark band on a bright background. In

Figure 9a, a dark, vertical bar is stationary in the center of the input image. Two vertical lines of dark pixels appear at the bar's edges. In Figure 9b, the bar is moving to the left: the right band of dark pixels widens, and the left band almost disappears. This verifies edge detection and motion enhancement. Nonuniformities and spuriously switched pixels evident in the images are manifestations of process nonuniformity and boundary effects at the edge of the resistive net.

Speed, power, concurrency, and scaling

We can appreciate the technology match between silicon CMOS and FLCs by looking at the energetics of SLM operation. Like fully complementary silicon CMOS circuitry, FLC modulator cells consume power only during switching transients. This means that total dissipated power varies linearly with the SLM frame rate. Frame rate is bounded by the heat removal capability of the SLM packaging; we express this condition as

$$f \times e_{sur} = p_{sur} < p_{pkg}$$

where f is the frame rate in Hz, e_{sur} is switching energy per unit area, p_{sur} is dissipated switching power per unit area, and p_{pkg} is the packaging-limited power dissipation per unit area. The energy required to switch a representative FLC cell operating in the visible spectrum is $e_{FLC} \approx 5 \text{ fJ}/\mu\text{m}^2$. Correspondingly, a minimum-geometry transistor in a modern VLSI process might have a gate capacitance of about 8 fF. Charging or discharging it through 5V requires an energy $E_{FET} \approx 0.1 \text{ pJ}$. To relate this energy to area, we use the transistor density of our retina arrays: 48 devices per $72\text{-}\mu\text{m} \times 62.4\text{-}\mu\text{m}$ cell, or 1 FET per $100 \mu\text{m}^2$. Thus, the area-specific switching energy of FETs in our arrays is about

$$e_{FET} = E_{FET}/100 \mu\text{m}^2 \approx 1 \text{ fJ}/\mu\text{m}^2$$

Acknowledging our use of larger-than-minimum-geometry transistors and conceding some static power dissipation to analog circuitry, we can infer that e_{FET} might realistically be a few times larger. In other words, the power dissipated by a FLC light-modulating layer is about the same as that of the CMOS circuitry beneath it.

There can be no better circumstance! Neither the FLC nor the silicon burdens the other with poorer speed-power performance. We can now make a thumbnail calculation of maximum frame rate for a dissipation of $100 \text{ mW}/\text{cm}^2$ (or $1 \text{ nW}/\mu\text{m}^2$), which is a comfortable regime for a device without explicit heat sinking:

$$f_{max} = (1 \text{ nW}/\mu\text{m}^2) / [(5 + 5) \text{ fJ}/\mu\text{m}^2] = 100 \text{ kHz}$$

In this scenario, we lose some (but not much) performance potential to the switching speed limitations of current FLC materials.

Estimates of the equivalent number of explicit computing operations performed by such devices as silicon retinas always give startlingly large numbers. Such high equivalent throughputs are partly due to the efficiency of purpose-designed hardware. Purpose-designed hardware exhibits high processing concurrency: a high fraction of transistors change state every cycle and thereby perform useful computation. A highly concurrent system can generate high computational throughput at modest clock rates.

The previous analysis hypothesized transistors and light modulators switching at the same rate. Performance scaling for such devices is trivial because they expend a fixed power per unit area at a given modulator switching rate, regardless of array size.

A qualitative difference exists in the scaling of devices whose transistors switch more frequently than their modulators, when the ratio depends on array size. Our electrically addressed SLMs are perfect examples: the Bit lines of an $N \times N$ device must cycle N times during one frame time (pixel-switching time). This tends to reduce the dissipation-limited frame rate because the circuitry becomes ever more power-hungry than the light modulators. Handschy et al.⁶ examines limits for the case of large, electrically addressed SLMs and concludes that $1,000 \times 1,000$ displays dissipating less than a watt can still frame at multi-kilohertz rates. In this case, FLC switching speed is not the limiting factor.

Finally, we touch on the constraint that the reliability hazard of metal migration eventually imposes on the permissible current density in power supply and global clocking conductors. Consider scaling an array that dissipates a constant power per unit area at constant aspect ratio (that is, such that the ratio of array width to array height is held constant). The total power and average total current rise quadratically with array diameter, while the area cross section of metal that must supply the current grows only linearly. Thus the current density in power and clock conductors grows linearly with array diameter. At present, silicon/FLC devices would have to dissipate multiple watts to encounter this limit. However, devices using a more power-hungry light modulator technology would encounter it sooner. Providing more heat-removal capacity does not solve the current density problem.

Assembly and packaging

It is not hard to make an optically marginal silicon/FLC device; it is very difficult to make a good one. Unlike twisted-nematic liquid crystal materials, the thickness of an FLC cell determines the amount of polarization rotation induced in modulation, and with it the achievable contrast. The FLC layer must therefore be of correct, uniform thickness across the device. Because this thickness is about $1 \mu\text{m}$, die bonding and window attachment processes are critical.

We fabricated early devices on die already packaged and wire-bonded according to standard practice. Measurements

on these parts typically showed deviations from flatness of more than a quarter wavelength of light. To overcome this problem, we developed a proprietary die attachment process that allows correction of some chip warpage.

The window is flat glass with an ITO transparent conductor on one side. We evaporate a metal contact onto an edge face of the window, which slightly overlaps the conductive layer to make electrical contact from the side. We can thus apply a bias voltage to the common electrode after assembly. We apply a thin-film polymer layer to the transparent conductor and rub it using a proprietary process. This induces proper alignment of the liquid crystal molecules in the surface-stabilized configuration.

A narrow fillet of ultraviolet-curable cement, which is deposited before contacting the surfaces, attaches the window to the die. A gap remains in the periphery to admit the liquid crystal, which is introduced under vacuum. The assembly is heated to well above the isotropic phase transition temperature of the FLC material. FLC is introduced at the cell edge and fills in by capillary action. The vacuum prevents air bubbles from forming near topographical features in the cell. After filling, the vacuum is released and the cell cooled slowly through any higher temperature phases to the ferroelectric phase at room temperature.

Outlook for gray-scale operation

We have thus far confined discussion in this article to binary light modulation; in their simple form, surface-stabilized FLC modulators are inherently bistable. Actually, there are several demonstrated prospects for obtaining gray-tone output from FLC light modulators.

One method does not actually employ partially transmitting cells, but uses the multi-kilohertz framing capability of electrically addressed silicon/FLC SLMs to display gray images. The method splits an image into binary planes, which are written sequentially to the device. The device then displays the least-significant plane for one unit of time, the next-least-significant plane for two units of time, and so on until it displays all planes with powers-of-two weighting. The human eye averages displayed intensity in this time-integration technique. Displaying a 7-bit-per-pixel image this way requires 255 minimum frame times and could be done in 25.5 ms on the Generation-3 SLM. Therefore, this approach is possible for television-bandwidth applications.

Another technique, charge-control domain switching, uses spatial averaging to modulate total instantaneous pixel output in the sense of a halftone image.⁷ A special surface preparation gives the cell a very fine-grained multidomain structure. Switching is still binary, but control of the exact charge driven into the pixel leads to switching of a well-defined number of domains that turn out to be quite uniformly distributed. For electrically addressed displays, the DRAM cell design is compatible with this technique in that

charging its storage capacitor quickly to a particular voltage meters a well-defined charge into the cell. The optically addressed devices we discussed are also amenable to this technique, because gating the current-source outputs of transconductance amplifiers onto FLC cells for a fixed, short interval does the same.

New liquid crystal materials embodying the deformable-helix ferroelectric effect are also amenable to charge-control switching.⁸ These materials provide true, spatially homogeneous, continuous modulation with low-voltage response times in the 100- μ s range. In cells made with these materials, charge is the variable most directly related to switching. This also means that light sensitivity is a prominent issue for DRAM SLMs using these materials.

SILICON VLSI CIRCUITRY AND FLCs are very well matched in terms of fabrication compatibility, operating voltage regime, and speed-power product. Using foundry silicon has many advantages. One is decoupling SLM functionality from physical design and packaging. Thus, once the fabrication process is developed for integrating the FLC light modulator layer with foundry die, a redesign of the chip can completely change the SLM's function without impacting the remainder of the process. Advances in silicon VLSI technology also become immediately available and can lead to rapid improvements. Features of modern, fine-line CMOS processes have clearly contributed to gains in the density, planarity, optical throughput, optical isolation, and performance of the devices presented here.

The convergence of device requirements for optical information display and processing will benefit both areas. Sophisticated technologies developed for information processing can contribute to the development of high-quality displays, and the economies of scale implied by a large display market will reduce the cost of SLMs for information processing. We foresee applications of silicon/FLC technology in areas where massive parallelism at moderate speeds and power dissipations is appropriate, such as in information display, special-purpose image processing, and robotic vision. There is yet significant potential for further extending the speed, resolution, and functionality of these devices. ■

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