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Ferroelectric liquid-crystal spatial light modulators for projection display

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We report prototype active-matrix liquid crystal spatial light modulators using ordinary silicon integrated-circuit backplanes and incorporating a fast-switching ferroelectric liquid crystal (FLC) light modulating layer at the backplane's surface. Backplanes reported here utilize a fully-planarized three-metal CMOS process for improved optical throughput, contrast, and light tolerance. We report a 256×256 device with $15 \mu\text{m}$ SRAM pixels having 87% fill-factor, optical throughput of 36–45%, contrast ratio of 80:1, and electrical rise/fall times of $85 \mu\text{s}$. We also report DRAM arrays with pixel pitches of $7.5 \mu\text{m}$ and $5.7 \mu\text{m}$, with fill factors of 75% and 69%, respectively.

Introduction. Projection displays serve a variety of application niches not filled by direct-view CRTs or flat-panel displays. Projectors offer screen diagonals larger than can be currently achieved with flat panels, at lower sizes and weights than feasible with direct-view CRTs. Especially promising are projectors based on “light valves” or spatial light modulators (SLMs), where the light generation and information formatting means are separated. One such SLM technology places a fast-switching ferroelectric liquid crystal (FLC) light modulating layer on an active-matrix backplane made from an ordinary CMOS silicon integrated circuit [1, 2]. FLCs are fast enough to favor field-sequential color and “digital” gray techniques, and are made in cells with gaps thin enough that pixel edge effects pose no practical limit to resolution. The multiple metal layers of standard CMOS processing enable reflective pixels with large aperture ratios undiminished by underlying pixel circuit complexity. These CMOS processes also have the capability to integrate high-speed interface circuitry and row/column drivers onto the display backplane. Backplane manufacture can be carried out in existing VLSI fabrication facilities, resulting in high-yield, low-cost devices. Final assembly into complete SLMs exploits mature, proven liquid-crystal display (LCD) manufacturing methodologies.

This approach to projection display faces its own challenges. Backplane surface topography resulting from standard VLSI processing techniques can degrade pixel mirror quality and result in inadequate optical throughput and contrast ratio. Since the underlying silicon substrate is optically thick, any light leaking through gaps between pixels is absorbed, and may result in photocurrents that degrade the performance of pixel circuitry. In this paper, we present prototype devices that overcome these challenges.

Prototype device design. An active-matrix display panel functions essentially as an electronic memory with optical readout. The backplane design can therefore be

pixel type:	SRAM	DRAM	DRAM
pixel pitch:	$15 \mu\text{m}$	$7.5 \mu\text{m}$	$5.7 \mu\text{m}$
gap width:	$1.0 \mu\text{m}$	$1.0 \mu\text{m}$	$1.0 \mu\text{m}$
fill factor:	87%	75%	69%

Table 1: Design characteristics of DRAM and SRAM pixels. Fill factors are computed from the inter-pixel gap dimension as drawn.

based on well-proven designs for silicon electronic memory. The simplest such memory cell is the one-transistor dynamic register that is the basis for dynamic random-access memory (DRAM). Electronic information in this register is stored as charge on a capacitor; information can be changed when the single transistor is turned on to connect the capacitor to a data line. The simplicity of this cell results in the most compact achievable layout, but inevitable backplane leakage currents across the memory capacitor require it to be periodically refreshed. The requirement for refresh is removed by the more complex static register; its standard form requires six transistors [3]. We have designed pixels using both DRAM and SRAM circuits, with the characteristics listed in Table 1. Our designs were carried out in a three-metal CMOS process with $0.8 \mu\text{m}$ ground rules. Even with the complexity of the SRAM pixel and the tight pitches of the DRAM pixels, smooth pixel-mirror surfaces were obtained by virtue of the reliance of the CMOS process on chemical-mechanical planarization whereby each intermetal dielectric layer is polished flat. Each pixel register is connected by a via to a metal pad fabricated in the third metal layer; this pad functions as both a pixel mirror and FLC drive electrode.

Complete SLMs were assembled from the CMOS chips using techniques similar to those reported previously [1]. An ITO-coated window carrying a rubbed nylon alignment layer was contacted to spacer posts fabricated by etching

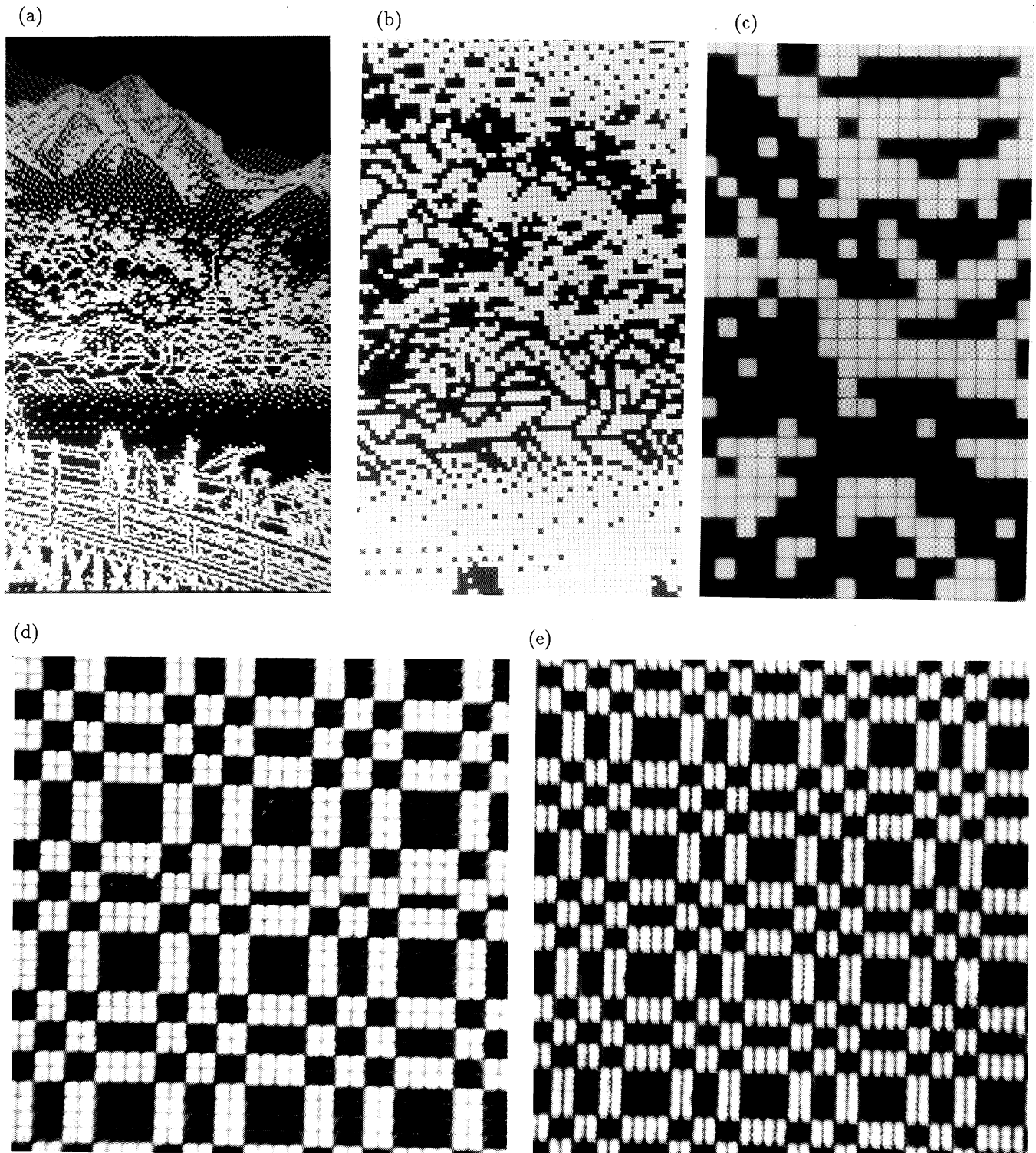


Figure 1: Photomicrographs of patterns written on SLMs: (a) 256×256 SRAM, nearly full aperture, (b)–(c) closeups of $15 \mu\text{m}$ SRAM pixels, (d) closeup of $7.5 \mu\text{m}$ DRAM pixels, (e) closeup of $5.7 \mu\text{m}$ DRAM pixels.

pixel type:	SRAM
rise/fall times (10/90%):	85 μ s
optical throughput:	
diffractive (zero order):	45%
diffuse (30° off-axis):	36%
contrast ratio:	
diffractive (zero order):	100:1
diffuse (30° off-axis):	80:1

Table 2: Measured performance of 256 \times 256 SRAM device.

the final oxide layer on the chip. Spacing was thus set to a value slightly less than 1 μ m, to give the device half-wave retardance for visible light after it was vacuum-filled with FLC material.

Results. Figure 1 shows photomicrographs of SRAM and DRAM pixel images. The SRAM device comprised a 256 \times 256 pixel array, about 3/4 of which is visible in Figure 1(a). At higher magnifications in Figures 1(b) and (c), the pixels are resolved, and can be seen to be essentially featureless by virtue of their planarization. The similarity between the dimension of the 1 μ m inter-pixel gap and the light wavelength ensures that the gap remains dark, giving a “seamless” appearance to regions of adjacent OFF pixels. These trends are preserved by the much tighter pitch DRAM pixels shown in Figure 1(d) and (e).

Other characteristics of the SRAM device performance are listed in Table 2. The table presents two distinctly different ways of optically characterizing such devices. The first characterizes the performance of the SLM in the way-most relevant to diffractive fourier optical systems. The characterization is carried out with the SLM illuminated by a collimated 633 nm HeNe laser beam. The beam is linearly polarized, and is incident on the SLM at a few degrees off normal. The reflection of the beam from the SLM produces a diffraction pattern in the far field; after passing the reflected light through an analyzer crossed to the polarization of the incident beam, the zero-order spot in this pattern is passed through an aperture and on to a photodetector. With the SLM oriented relative to the incident polarization for maximum contrast, we measure the detected intensity when the SLM is written all-ON and all-OFF. Analyzer losses are normalized out by assigning to the incident beam intensity the detector value measured with a high-reflectivity mirror substituted for the SLM and the analyzer set parallel to the incident polarization. Using this protocol, the SRAM device diffracted 45% of the incident light into the zero order, and achieved an all-ON/all-OFF contrast ratio of 100:1.

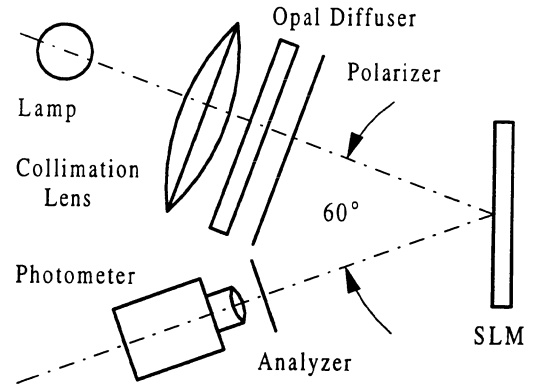


Figure 2: SLM characterization for imaging applications.

The second way of optically characterizing the device is more appropriate for applications such as projection display where the SLM is imaged. In this case, the all-ON and all-OFF intensities are measured using the set-up shown in Figure 2. Here the light source is an opal-glass diffuser illuminated by white light from an incandescent bulb, and the detector is a photometer. The photometer was positioned so the detected light was reflected from the SLM at an angle 30° to the SLM normal. Correcting for polarizer and analyzer losses in the same way as before, the ON-state throughput measured 35%, with an ON/OFF contrast ratio of 80:1. We intend to carry out more complete characterizations over a range of incidence and azimuthal polarization angles.

Conclusions. We have demonstrated SLMs with characteristics useful for projection displays. SRAM pixels confer the maximum light tolerance, while DRAM pixels enable the highest resolutions. In either case, the use of planarization results in pixel mirrors with high optical quality. We estimate that further layout optimization could shrink the

pixel type:	SRAM	SRAM	DRAM
VLSI rule:	0.8 μ m	0.6 μ m	0.8 μ m
pixel pitch:	12 μ m	9 μ m	7.5 μ m
fill factor:	84%	84%	75%
resolution	array dimensions (mm)		
640 \times 480	7.7 \times 5.8	5.8 \times 4.3	4.8 \times 3.6
800 \times 600	9.6 \times 7.2	7.2 \times 5.4	6.0 \times 4.5
1024 \times 768	12.3 \times 9.2	9.2 \times 6.9	7.7 \times 5.8
1280 \times 1024	15.4 \times 12.3	11.5 \times 9.2	9.6 \times 7.7
2048 \times 1536	24.6 \times 18.4	18.4 \times 13.8	15.4 \times 11.5

Table 3: Feasible array sizes for various VLSI design rules and pixel types.

pitch of the SRAM pixels to $12\ \mu\text{m}$ using the same $0.8\ \mu\text{m}$ design rules. Finer-line processes are now widely available; the use of, for example, a $0.6\ \mu\text{m}$ process would allow SRAM pixels on $9\ \mu\text{m}$ centers. The array sizes for a variety of display formats and pixel types are summarized in Table 3. At the lowest resolutions, the array sizes are probably too small, even with the coarser SRAM pixels, for efficient illumination by available arc lamps. The larger array sizes, however, can be illuminated efficiently, and will clearly enable displays with very high resolutions.

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