Technical Note

Comparing 128Mb P8P Parallel PCM and Parallel NOR Flash Memory

Introduction

The purpose of this technical note is to compare features of the 128Mb P8P parallel PCM and parallel NOR Flash memory devices. Features compared include memory architecture, package options, signal descriptions, command sets, electrical specifications, and device identification, software, and performance.

Features of Phase Change Memory

Bit Alterability

Phase change memory (PCM) has bit alterability, which is the ability to change each memory bit independently from 0 to 1 or 1 to 0 without an intervening BLOCK ERASE operation. Bit alterability enables software to write to the nonvolatile memory in the same way that writing to RAM or EEPROM eliminates the overhead of erasing blocks prior to write. Bit-alterable WRITEs use the same command sequences as a traditional buffered program sequence.

P8P parallel PCM devices have a set of bit-alterable WRITE commands that use the same sequences as page program sequences. The primary difference with the bit-alterable commands in P8P parallel PCM devices is that when the device starts executing, the data written to the buffer is directly overwritten into the P8P parallel PCM device, unlike Flash memory, which can only go from 1 to 0 before an erase of the entire block.

For highest program performance, P8P parallel PCM devices have a bit-alterable program on all 1s commands that enables the device to program at higher performance when the locations in the addressed page have previously been set (1s).

Unlike floating gate Flash memory, P8P parallel PCM devices do not require a high-voltage BLOCK ERASE operation to change all bits in a block to 1. As a bit-alterable technology, each bit can be independently changed from 0 to 1 and from 1 to 0. To maintain compatibility with legacy Flash system software, P8P parallel PCM devices mimic or emulate a Flash erase by writing each bit in a block to 1.

Bit alterability minimizes system overhead for software management of data and ultimately improves latency and determinism and reduces power consumption. Storing counter variables can be easily handled using PCM memory because a 0 can change to a 1 or a 1 can change to a 0.

Endurance

P8P parallel PCM devices are capable of more than 1 million WRITE cycles, demonstrating better endurance than NAND or NOR Flash devices. Endurance is different than with traditional nonvolatile memory because a PCM WRITE cycle is defined as any time a bit changes within a 32-byte page.

Performance

P8P parallel PCM devices deliver better performance from system memory because they provide faster programming and erase speeds than traditional NOR Flash technology. P8P parallel PCM devices accomplish this while maintaining compatibility with legacy Flash system software by having the same command sets and emulating Flash erase.

Memory Array Architecture

Table 1: Memory Array Architecture

P8P Parallel PCM	Parallel NOR Flash Memory
Asymmetrical block architecture: Four 32KB parameter blocks (top or bottom configuration) 128KB main blocks	Asymmetrical block architecture (P30/P33): Four 32KB parameter blocks (top or bottom configuration) 128KB main blocks
N/A	Symmetrical block architecture (J3): 128KB main blocks

Package Configurations

Table 2: Package Configurations

Package	P8P Parallel PCM	P30	P33	J3
56-pin TSOP	14mm x 20mm	14mm x 20mm	14mm x 20mm	14mm x 20mm
Easy BGA	10mm x 8mm	10mm x 13mm	10mm x 8mm	10mm x 13mm

1. Refer to the P8P parallel PCM and parallel NOR Flash data sheets for package details and pinout comparisons.

Signal Descriptions

Signal compatibility between P8P parallel PCM and parallel NOR Flash devices is shown in the Signal Description table. Note that P8P parallel PCM devices have SPI signals that enable the devices to be placed in a serial interface mode for preprogramming, while parallel NOR Flash devices do not support this mode. Parallel NOR Flash has ADV#, CLK, BYTE#, STS, VPEN, and WAIT signals that are not supported on P8P parallel PCM devices.

Table 3: Signal Descriptions

P8P Parallel PCM Signal	Parallel NOR Flash Signal	Type	Description
N/A	A0	Input	**Byte-select address**: Selects between HIGH and LOW byte when the device is in x8 mode. This address is latched during a x8 PROGRAM cycle, but is not used in x16 mode. (For example, the A0 input buffer is turned off when BYTE# is HIGH.)
A[MAX:1]	A[MAX:1]	Input	**Address inputs**: Device address inputs. 256Mb: A[24:1]; 128Mb: A[23:1]; 64Mb: A[22:1]. Note: The address bus for TSOP and Easy BGA starts at A1. P8P parallel PCM uses x16 addressing, but the package is x8 addressing to ensure compatibility with parallel NOR Flash memory products.
DQ[15:0]	DQ[15:0]	Input/Output	**Data input/output**: Inputs data and commands during WRITEs (internally latched). Outputs data during READ operations. Data signals float when CE# or OE# are V_{IH} or RST# is V_{IL}.
N/A	DQ[7:0]	Input/Output	**Low byte data bus**: Inputs data during buffer writes and programming and inputs commands during CUI writes. Outputs array, CFI, identifier, or status data in the appropriate read mode. Data is internally latched during WRITE operations.
N/A	DQ[15:8]	Input/Output	**High byte data bus**: Inputs data during x16 buffer writes and PROGRAMMING operations. Outputs array, CFI, or identifier data in the appropriate read mode; not used for status register reads. Data is internally latched during WRITE operations in x16 mode; [15:8] float in x8 mode.
N/A	ADV#	Input	**Address valid**: Active LOW input. During synchronous READ operations, addresses are latched on the rising edge of ADV# or on the next valid CLK edge with ADV# LOW, whichever occurs first. In asynchronous mode, the address is latched when ADV# going HIGH or continuously flows through if ADV# is held LOW. Note: Designs not using ADV# must tie it to V_{SS} to enable addresses to flow through.
CE# or S#	CE#	Input or SPI	**Chip enable**: CE# LOW activates internal control logic, I/O buffers, decoders, and sense amps. CE# HIGH deselects the device, places it in standby state, and places data outputs in High-Z. **SPI select**: S# LOW activates WRITE command to the SPI interface. Rising S# to V_{IH} completes (or terminates) the SPI command cycle; it also sets Q to High-Z.
N/A	CLK	Input	**Clock**: Synchronizes the device with the system's bus frequency in synchronous read mode. During synchronous READ operations, addresses are latched on the rising edge of ADV# or on the next valid CLK edge with ADV# LOW, whichever occurs first. Note: Designs not using CLK for synchronous read mode must tie it to V_{CCQ} or V_{SS}.

Table 3: Signal Descriptions (continued)

P8P Parallel PCM Signal	Parallel NOR Flash Signal	Type	Description
OE# or HOLD#	OE#	Input or SPI	**Output enable**: Active LOW OE# enables the output data buffers during a READ cycle. With OE# at V_{IH}, device data outputs are placed in High-Z. **SPI HOLD#**: When asserted, suspends the current cycle and sets Q to High-Z until de-asserted.
RST#	RST#/RP#	Input	**Reset chip**: When LOW, RST# resets internal automation and inhibits WRITE operations. This provides data protection during power transitions. RST# HIGH enables normal operation. The device is in 8-word page mode array read after reset exits.
N/A	WAIT	Output	**Wait**: Indicates data valid in synchronous array or nonarray burst reads. RCR[10], (WT), determines its polarity when asserted. WAIT active output is V_{OL} or V_{OH} when CE# and OE# are V_{IL}. WAIT is High-Z if CE# or OE# are V_{IH}. In synchronous array or nonarray read modes, WAIT indicates invalid data when asserted and valid data when de-asserted. In asynchronous page mode and all write modes, WAIT is de-asserted.
WE#	WE#	Input	**Write enable**: Active LOW input. WE# controls writes to the device. Address and data are latched on the rising edge of WE#.
WP#	WP#	Input	**Write protect**: Active LOW input. WP# LOW enables the lock down mechanism. Blocks in lock down cannot be unlocked with the UNLOCK command. WP# HIGH overrides the lock down function, enabling blocks to be erased or programmed using software commands.
N/A	STS	Open-drain output	**Status**: Indicates the status of the internal state machine. When configured in level mode (default), it acts as an RY/BY# signal. When configured in one of its pulse modes, it can pulse to indicate program and/or erase completion. STS must be tied to V_{CCQ} with a pull-up resistor.
N/A	BYTE#	Input	**Byte enable**: BYTE# LOW places the device in x8 mode; data is input or output on D[7:0], while D[15:8] is placed in High-Z. Address A0 selects between the HIGH and LOW byte. BYTE# HIGH places the device in x16 mode and turns off the A0 input buffer. The address A1 becomes the lowest order address bit.
N/A	VPEN	Input	**Erase/program/block lock enable**: Used for erasing array blocks, programming data, or configuring lock bits. With VPEN ≤ VPENLK, memory contents cannot be altered.
C	N/A	SPI	**SPI clock**: Synchronization clock for input and output data.
D	N/A	SPI	**SPI data input**: Serial data input for op codes, address, and program data bytes. Input data is clocked in on the rising edge of C, starting with the MSB.
Q	N/A	SPI	**SPI data output**: Serial data output for read data. Output data is clocked out, triggered by the falling edge of C, starting with the MSB.
SERIAL	N/A	SPI	**SPI enable**: SERIAL is a port-select switching between the normal parallel or serial interface. When V_{SS}, the normal (non-SPI) P8P parallel PCM interface, is enabled, all other SPI inputs are "Don't Care," and Q is High-Z. When V_{CC} SPI mode is enabled, all non-SPI inputs are Don't Care, and all outputs are High-Z. This pin has an internal weak pull-down resistor to select the normal parallel interface when users leave the pin floating. A CAM can be used to permanently disable this feature.
V_{PP}	V_{PP}	Power	**Erase and write power**: A valid V_{PP} voltage enables erase or programming. Memory contents can't be altered when $V_{PP} \leq$ to V_{PPLK}. Set $V_{PP} = V_{CC}$ for in-system PROGRAM and ERASE operations. To accommodate resistor or diode drops from the system supply, the V_{PP} V_{IH} level can be as low as $V_{PPL,min}$. Program/erase voltage is normally 1.7V to 3.6V.

Table 3: Signal Descriptions (continued)

P8P Parallel PCM Signal	Parallel NOR Flash Signal	Type	Description
V_{CC}	V_{CC}	Power	**Device power supply**: Writes are inhibited at $V_{CC} \leq V_{LKO}$. Device operations at invalid V_{CC} voltages should not be attempted.
V_{CCQ}	V_{CCQ}	Power	**Output power supply**: Enables all outputs to be driven at V_{CCQ}. This input may be tied directly to V_{CC} if V_{CCQ} is to function within the V_{CC} range.
V_{SS}	V_{SS}	Power	**Ground**: Connects device circuitry to system ground.
V_{SSQ}	N/A	Power	**I/O ground**: Tie to GND.
RFU	RFU	–	**Reserved for future use**: Do not connect to other signals.
DU	DU	–	**Don't use**: Do not connect to power supply or other signals.
NC	NC	–	**No connect**: No internal connection; can be driven or floated.

Commands

Table 4: Supported Command Set

Command Name	P8P Parallel PCM Command Code	Parallel NOR Flash Command Code	Notes
READ			
READ ARRAY	FFh	FFh	1
READ STATUS REGISTER	70h	70h	
READ ID CODE	90h	90h	
READ QUERY	98h	98h	
CLEAR STATUS REGISTER	50h	50h	
PROGRAM			
PROGRAM SETUP	40h/10h	40h	
BIT ALTERABLE WRITE	42h	N/A	2
BUFFERED PROGRAM	E8h	E8h	
BIT ALTERABLE BUFFERED PROGRAM	EAh	N/A	2
BUFFERED PROGRAM (on all 1s)	DEh	N/A	2
BEFP SETUP	N/A	80h	3
BUFFERED WRITE CONFIRM	D0h	D0h	
ERASE			
BLOCK ERASE SETUP	20h	20h	
ERASE CONFIRM	D0h	D0h	
SUSPEND			
WRITE SUSPEND	B0h	B0h	4
ERASE SUSPEND	B0h	B0h	4
SUSPEND RESUME	D0h	D0h	4
BLOCK LOCKING			
LOCK SETUP	60h	60h	
LOCK BLOCK	01h	01h	
UNLOCK BLOCK	D0h	D0h	
LOCK DOWN	2Fh	2Fh	

Notes:
1. The READ ARRAY command places the device in read array mode. Upon initial device power-up or after a reset, the device defaults to read array mode.
2. Not supported on parallel NOR Flash devices.
3. Not supported on P8P parallel PCM devices.
4. For AC/DC specifications, refer to the product data sheets.

PROGRAM Commands

P8P parallel PCM and parallel NOR Flash devices support buffered program commands. In addition, P8P parallel PCM devices have a set of bit-alterable WRITE commands, which have the same sequences as the BUFFER PROGRAM commands. The primary difference with the bit-alterable commands in P8P parallel PCM devices is that when the write state machine starts executing, the data written to the buffer is directly overwritten into the P8P parallel PCM device, unlike Flash memory, which can only go from 1 to 0 before an erase of the entire block.

P8P parallel PCM devices have a bit-alterable buffered program on all the 1s command (DEh) that enables the device to program at higher performance when the locations in the addressed page have previously been set (1s).

ERASE Commands

Unlike floating gate Flash memory, P8P parallel PCM devices do not require a high-voltage BLOCK ERASE operation to change all the bits in a block to 1. As a bit-alterable technology, each bit is capable of being independently changed from a 0 to a 1 and from a 1 to a 0.

To maintain compatibility with legacy Flash system software, P8P parallel PCM devices mimic or emulate a Flash erase by writing each bit in a block to 1.

Electrical Characteristics

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to operating conditions for extended periods may adversely affect reliability.

Operating Conditions

Table 5: Operating Conditions

Parameter		Symbol	P8P Parallel PCM		Parallel NOR Flash		Unit
			Min	Max	Min	Max	
Operating temperature[1]		T_C	–40	85	–40	85	°C
V_{CC} supply voltage		V_{CC}	2.7	3.6	2.3	3.6	V
I/O supply voltage	CMOS input	V_{CCQ}	1.7	3.6	2.3	3.6	V
	TTL input		2.4	3.6	2.4	3.6	
V_{PP} supply voltage		V_{PP}	0.9	3.6	1.5	3.6	V
Buffered enhanced factory program V_{PP}		V_{PPH}	N/A	N/A	8.5	9.5	V
V_{PPH} time		^tPPH	–	N/A	–	80	Hours
Main block		WRITE cycles[2]	1 million[3]	–	100,000[4]	–	Cycles
Parameter block							

Notes:
1. Case temperature.
2. In typical operation where $V_{PP} = V_{PPL}$.
3. P8P parallel PCM WRITE cycles are defined as any time a bit changes within a 32-byte page.
4. NOR Flash WRITE cycles are defined as the program/erase of a block.

DC Specifications

Table 6: DC Current Specifications

Parameter	Symbol	P8P Parallel PCM (2.4–3.6V)		Parallel NOR Flash[1] (2.4–3.6V)		Unit
		Typ	Max	Typ	Max	
Standby current	I_{CCS}	80	160	55–65	120–210	µA
Read current (async single word)	I_{CCR}	30	42	20–26	25–31	mA
Read current (page mode)	I_{CCR}	15	20	12	16	mA
Write current	I_{CCW}	36	51	35	50	mA
Erase current	I_{CCE}					

Notes: 1. Parallel NOR Flash values represent a range of 65nm SLC (128Mb) and MLC (256Mb) devices.

Table 7: DC Voltage Specifications

Parameter	Symbol	P8P Parallel PCM (2.4–3.6V)		Parallel NOR Flash[1] (2.4–3.6V)		Unit
		Min	Max	Min	Max	
Input low voltage	V_{IL}	0	0.6	–0.5	0.6	V
Input high voltage	V_{IH}	2.0	V_{CCQ}	2.0	V_{CC} + 0.5	V
Output low voltage[2]	V_{OL}	–	0.1	–	0.2	V
Output high voltage[3]	V_{OH}	V_{CCQ} - 0.1	–	V_{CCQ} - 0.1	–	V
V_{CC} lockout voltage	V_{LKO}	1.5	–	1.5	–	V
V_{CCQ} lockout voltage	V_{LKOQ}	0.9	–	0.9	–	V

Notes: 1. Parallel NOR Flash values represent a range of 65nm SLC (128Mb) and MLC (256Mb) devices.
2. Test condition is $V_{CC} = V_{CC,min}$; $V_{CCQ} = V_{CCQ,min}$; I_{OL} = 100µA.
3. Test condition is $V_{CC} = V_{CC,min}$; $V_{CCQ} = V_{CCQ,min}$; I_{OH} = 100µA.

Reset Specifications

Table 8: DC Power and Reset Specifications

Number	Parameter	Symbol	P8P Parallel PCM		Parallel NOR Flash[1]		Unit
			Min	Max	Min	Max	
P1	RST# pulse width low	^tPLPH	100	–	100	–	ns
P2	RST# low to device reset during erase	^tPLRH	–	40	–	25	µs
	RST# low to device reset during erase		–	40	–	25	µs
P3	V_{CC} power valid to RST# de-assertion (HIGH)	^tVCCPH	100	–	60–300	–	µs

Notes: 1. Parallel NOR Flash values represent a range of 65nm SLC (128Mb) and MLC (256Mb) devices.

Table 9: AC READ Specifications

Parameter	Symbol	P8P Parallel PCM		Parallel NOR Flash[1]		Unit
		Min	Max	Min	Max	
Read cycle time (0°C to 70°C)	^{t}AVAV	115	–	60–70	–	ns
Address to output valid (0°C to 70°C)	^{t}AVQV	–	115	–	60–70	ns
CE# LOW to output valid (0°C to 70°C)	^{t}ELQV	–	115	–	60–70	ns
Read cycle time (–40°C to 85°C)	^{t}AVAV	115	–	135	–	ns
Address to output valid (–40°C to 85°C)	^{t}AVQV	–	115	–	135	ns
CE# LOW to output valid (–40°C to 85°C)	^{t}ELQV	–	115	–	135	ns
OE# LOW to output valid	^{t}GLQV	–	25	–	25	ns
RST# HIGH to output valid	^{t}PHQV	–	150	–	150	ns
CE# LOW to output in Low-Z	^{t}ELQX	0	–	0	–	ns
OE# LOW to output in Low-Z	^{t}GLQX	0	–	0	–	ns
CE# HIGH to output in High-Z	^{t}EHQZ	–	24	–	20	ns
OE# HIGH to output in High-Z	^{t}GHQZ	–	24	–	15	ns
Output HOLD from first occurring address, CE#, or OE# change	^{t}OH	0	–	0	–	ns
CE# pulse width high	^{t}EHEL	20	–	17	–	ns
Page address access	^{t}APA	–	25	–	25	ns

Notes:
1. Parallel NOR Flash values represent a range of 65nm SLC (128Mb) and MLC (256Mb) devices.
2. AC specifications compare the fastest versions available at the full voltage range (2.7–3.6V). For the complete list of AC specifications, refer to the product data sheets.
3. P8P parallel PCM devices do not support synchronous burst reads.

Table 10: AC WRITE Specifications

Parameter	Symbol	P8P Parallel PCM		Parallel NOR Flash[1]		Unit
		Min	Max	Min	Max	
RST# HIGH recovery to WE# LOW	^{t}PHWL	150	–	150	–	ns
CE# setup to WE# LOW	^{t}ELWL	0	–	0	–	ns
WE# WRITE pulse width LOW	^{t}WLWH	50	–	50	–	ns
Data setup to WE# HIGH	^{t}DVWH	50	–	50	–	ns
Address valid setup to WE# HIGH	^{t}AVWH	50	–	50	–	ns
CE# hold from WE# HIGH	^{t}WHEH	0	–	0	–	ns
Data hold from WE# HIGH	^{t}WHDX	0	–	0	–	ns
Address hold from WE# HIGH	^{t}WHAX	0	–	0	–	ns
WE# pulse width HIGH	^{t}WHWL	20	–	20	–	ns
V_{PP} setup to WE# HIGH	^{t}VPWH	200	–	200	–	ns
V_{PP} hold from valid status read	^{t}QWL	0	–	0	–	ns
WP# hold from valid status read	^{t}QVBL	0	–	0	–	ns
WP# setup to WE# HIGH	^{t}BHWH	200	–	200	–	ns
WE# HIGH to OE# LOW	^{t}WHGL	0	–	0	–	ns

Table 10: AC WRITE Specifications (continued)

Parameter	Symbol	P8P Parallel PCM		Parallel NOR Flash[1]		Unit
		Min	Max	Min	Max	
WE# HIGH to read valid	^{t}WHQV	^{t}AVQV + 35	–	^{t}AVQV + 35	–	ns
WE# HIGH to address valid	^{t}WHAV	0	–	0	–	ns

Notes: 1. Parallel NOR Flash values represent a range of 65nm SLC (128Mb) and MLC (256Mb) devices.
2. P8P parallel PCM devices do not support write to synchronous burst reads.

Program and Erase Specifications

Table 11: Program and Erase Specifications

Parameter	Symbol	P8P Parallel PCM		Parallel NOR Flash		Unit
		Typ	Max	Typ	Max	
ERASE or ERASE-RESUME to ERASE-SUSPEND	^{t}ERS/SUSP	500	–	500	–	µs
WRITE SUSPEND	^{t}SUSP/P	35	60	15–20	20–25	µs
ERASE SUSPEND	^{t}SUSP/E	35	60	15–20	20–25	µs
Erase time (32Kb parameter)	^{t}ERS/PB	100	200	400–800	2500–4000	ms
Erase time (128Kb main)	^{t}ERS/MB	400	800	500–800	4000	µs
Single word program (legacy program and bit-alterable write	^{t}PROG/W	120	240	40–150	175–456	µs
Buffer program time (64 bytes) with legacy program or bit-alterable write	^{t}PROG/PB	120	360	53–176	200–716	µs
Buffer program time (64 bytes) with program on all 1's write		71	280	N/A	N/A	µs

Device Identification

Manufacturer identification is assigned by JEDEC. As a result, the P8P parallel PCM and parallel NOR Flash memory devices have the same manufacturer ID but different device ID codes. Both devices use command 90h to read these codes.

Table 12: P8P Parallel PCM Read Identification Summary

Parameter	P8P Parallel PCM Code
Manufacturer	0089h
Device ID (top)	881Eh
Device ID (bottom)	8821h

Conclusion

Comparing the features of the 128Mb P8P parallel PCM and parallel NOR Flash memory devices enables users to migrate applications from NOR Flash to P8P parallel PCM.

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