



Technical Note

Migrating from Macronix's MX25L25635E to Micron's N25Q 256Mb Flash Devices

Introduction

The purpose of this technical note is to compare features of the Micron® N25Q (256Mb) and Macronix MX25L25635E Flash memory devices. Features compared include memory architecture, package options, signal descriptions, command sets, electrical specifications, and device identification.



Memory Array Architecture

N25Q Features	MX25L Features
Program 1 to 256 bytes	Program 1 to 256 bytes
Uniform sector erase (64KB)	Uniform sector erase (32KB and 64KB)
Uniform subsector erase (4KB)	Uniform subsector erase (4KB)

Package Configurations

Table 1: Package Configurations

Package	N25Q 256Mb	MX25L25635E
V-PDFN8 (8mm x 6mm)	Yes	Yes
SOP2-16/300 mil	Yes	Yes
T-PBGA24 (6mm x 8mm)	Yes	–

Signal Descriptions

Table 2: Signal Descriptions

N25Q Signal	MX25L Signal	Type	Description
C	SCLK	Input	Serial clock
DQ0	SI/SIO0	Input or I/O	Serial data input or I/O
DQ1	SI/SIO0/P07	Output or I/O	Serial data output or I/O
S#	CS#	Input	Chip select
W/V _{pp} /DQ2	#WP/SIO2	Input or I/O	Write protect/enhanced program supply voltage or I/O
HOLD#/DQ3	HOLD/RESET/SIO3	Input or I/O	HOLD or I/O
V _{CC}	V _{CC}	Input	Supply voltage
V _{SS}	GND	Input	Ground

The MX25L device does not support enhanced program supply voltage (V_{pp} signal). During quad I/O operation, the MX25L device must set a bit (QE in SR6) for quad I/O functionality.

The N25Q device must set a bit (VCR or NVCR) for quad or dual protocols. During QSPI protocol, the W and HOLD signals are not available.



Commands

Table 3: Command Set

Command	Command Code N25Q	Command Code MX25L25635E	Notes
RESET Operations			
RESET ENABLE	66h	N/A	
RESET MEMORY	99h	N/A	
IDENTIFICATION Operations			
READ ID	9E/9Fh	9Fh	
MULTIPLE I/O READ ID	AFh	N/A	
READ ELECTRONIC SIGNATURE	N/A	ABh/90h	
READ ID (2x I/O, 4x I/O)	N/A	EFh/DFh	
READ SERIAL FLASH DISCOVERY PARAMETER	5Ah	N/A	
READ Operations			
READ	03h	03h	
FAST READ	0Bh	0Bh	
DUAL OUTPUT FAST READ	3Bh	3Bh	
DUAL INPUT/OUTPUT FAST READ	BBh	BBh	
QUAD OUTPUT FAST READ	6Bh	6Bh	
QUAD INPUT/OUTPUT FAST READ	EBh	EBh	
FAST READ . DTR	0Dh	N/A	
DUAL OUTPUT FAST READ . DTR	3Dh	N/A	
DUAL INPUT/OUTPUT FAST READ . DTR	BDh	N/A	
QUAD OUTPUT FAST READ . DTR	6Dh	N/A	
QUAD INPUT/OUTPUT FAST READ . DTR	EDh	N/A	
4-BYTE READ	13h	N/A	
4-BYTE FAST READ	0Ch	N/A	
4-BYTE DUAL OUTPUT FAST READ	3Ch	N/A	
4-BYTE DUAL INPUT/OUTPUT FAST READ	BCh	N/A	
4-BYTE QUAD OUTPUT FAST READ	6Ch	N/A	
4-BYTE QUAD INPUT/OUTPUT FAST READ	ECh	N/A	
WRITE Operations			
WRITE ENABLE	06h	06h	
WRITE DISABLE	04h	04h	
REGISTER Operations			
READ STATUS REGISTER	05h	05h	
WRITE STATUS REGISTER	01h	01h	
READ LOCK REGISTER	E8h	N/A	
WRITE LOCK REGISTER	E5h	N/A	
READ FLAG STATUS REGISTER	70h	N/A	



Table 3: Command Set (Continued)

Command	Command Code N25Q	Command Code MX25L25635E	Notes
CLEAR FLAG STATUS REGISTER	50h	N/A	
READ NONVOLATILE CONFIGURATION REGISTER	B5h	N/A	
WRITE NONVOLATILE CONFIGURATION REGISTER	B1h	N/A	
READ VOLATILE CONFIGURATION REGISTER	85h	N/A	
WRITE VOLATILE CONFIGURATION REGISTER	81h	N/A	
READ ENHANCED VOLATILE CONFIGURATION REGISTER	65h	N/A	
WRITE ENHANCED VOLATILE CONFIGURATION REGISTER	61h	N/A	
READ EXTENDED ADDRESS REGISTER	C8h	N/A	
WRITE EXTENDED ADDRESS REGISTER	C5h	N/A	
READ SECURITY REGISTER	N/A	2Bh	
WRITE SECURITY REGISTER	N/A	2Fh	
CLEAR SECURITY REGISTER FAIL FLAG	N/A	30h	
PROGRAM Operations			
PAGE PROGRAM	02h	02h	
CONTINUOUS PROGRAM	N/A	ADh	
ESRY	N/A	70h	
DSRY	N/A	80h	
DUAL INPUT FAST PROGRAM	A2h	N/A	
EXTENDED DUAL INPUT FAST PROGRAM	D2h	N/A	
QUAD INPUT FAST PROGRAM	32h	38h	
EXTENDED QUAD INPUT FAST PROGRAM	12h	N/A	
ERASE Operations			
4KB SUBSECTOR ERASE	20h	20h	
32KB SUBSECTOR ERASE	N/A	52h	
SECTOR ERASE	D8h	D8h	
BULK ERASE	C7h	60h/C7h	
PROGRAM/ERASE RESUME	7Ah	N/A	
PROGRAM/ERASE SUSPEND	75h	N/A	
ONE-TIME PROGRAMMABLE (OTP) Operations			
READ OTP ARRAY	4Bh	N/A	
PROGRAM OTP ARRAY	42h	N/A	
ENTER SECURED OTP	N/A	B1h	1
EXIT SECURED OTP	N/A	C1h	1
WRITE PROTECTION SELECTION	N/A	68h	2
SINGLE BLOCK LOCK	N/A	36h	3
SINGLE BLOCK UNLOCK	N/A	39h	3

Table 3: Command Set (Continued)

Command	Command Code N25Q	Command Code MX25L25635E	Notes
BLOCK PROTECT READ	N/A	3Ch	
GANG BLOCK LOCK	N/A	7Eh	
GANG BLOCK UNLOCK	N/A	98h	
4-BYTE ADDRESS MODE Operations			
ENTER 4-BYTE ADDRESS MODE	B7h	B7h	
EXIT 4-BYTE ADDRESS MODE	E9h	E9h	
DEEP POWER-DOWN			
DEEP POWER-DOWN	B9h	B9h	4
RELEASE FROM DEEP POWER-DOWN	ABh	ABh	4

- Notes:
1. These commands are not necessary for enabling access to the OTP array (64B instead of 4Kb, such as in the MCIX device). N25Q is featured with READ OTP/PROGRAM OTP specific commands
 2. SRAM bits are equivalent to N25Q lock registers. Compared to MX25L SRAM bits, which are enabled by WRITE PROTECTION SELECTION commands, N25Q lock registers are always available, regardless of the BPx bit status, and are enabled by READ/WRITE LOCK REGISTERS commands.
 3. Same result using WRITE LOCK REGISTER command.
 4. DEEP POWER-DOWN operation is only available in N25Q 1.8V devices.

Table 4: Different Commands Sharing Same Command Code

Command Code	N25Q 256Mb Command	MX25L25635E Command
ABh	RELEASE FROM DEEP POWER DEEP	RELEASE FROM DEEP POWER DEEP/ READ ELECTRONIC ID
70h	CLEAR FLAG STATUS REGISTER	ESRY
B1h	WRITE NONVOLATILE CONFIGURATION REGISTER	ENTER SECURED OTP
3Ch	4-BYTE DUAL OUTPUT FAST READ	BLOCK PROTECT READ

READ Commands

The READ command set for the N25Q and MX25L devices is identical, and each device follows the standard three address byte protocol.

The MX25L has a fixed dummy cycle read, but the N25Q dummy cycles can be configured and controlled in the nonvolatile configuration register (NVCR), bits 12 to 15, or in the volatile configuration register (VCR), bits 7 to 4.

MX25L requires a nonvolatile QE bit in the SR2 to enable the quad I/O functionality, and when this bit is set, the W pin is disabled.

VECR or NVCR enables the QSPI protocol (refer to the data sheet for more details). QUAD commands are available without any register setting. When VECR or NVCR bits are set, W and HOLD are still functional. With NVCR set (bit 3 = 0), the device can be



powered up or down with quad I/O functionality. No additional commands are required for N25Q to use quad or dual I/O functionality.

The MX25L and N25Q manufacturer ID, memory type, and memory capacity can be read out by issuing a 9Fh command. N25Q will output the same data when the 9Eh command is issued.

The MX25L device has commands that output the device ID (ABh), and a command that outputs the manufacturer ID and device ID (90h).

Power-Up Commands

MX25L requires power-up to have a certain V_{CC} slope and stay within the V_{CC} rise time specification (t_{VR}). N25Q has no power-up limitation and can speed up the power-on sequence.

Execute in Place (XIP)

The protocol for execute in place (XIP) is different for the two devices. N25Q XIP is configured by selecting the appropriate line item or by issuing the correct confirmation command, whereas the MX25L XIP is enabled by issuing the correct confirmation command. Refer to Application Note, "Using XIP Modes in the Forte™ N25Q Flash Memory Device."

Figure 1: XIP Timing Configuration

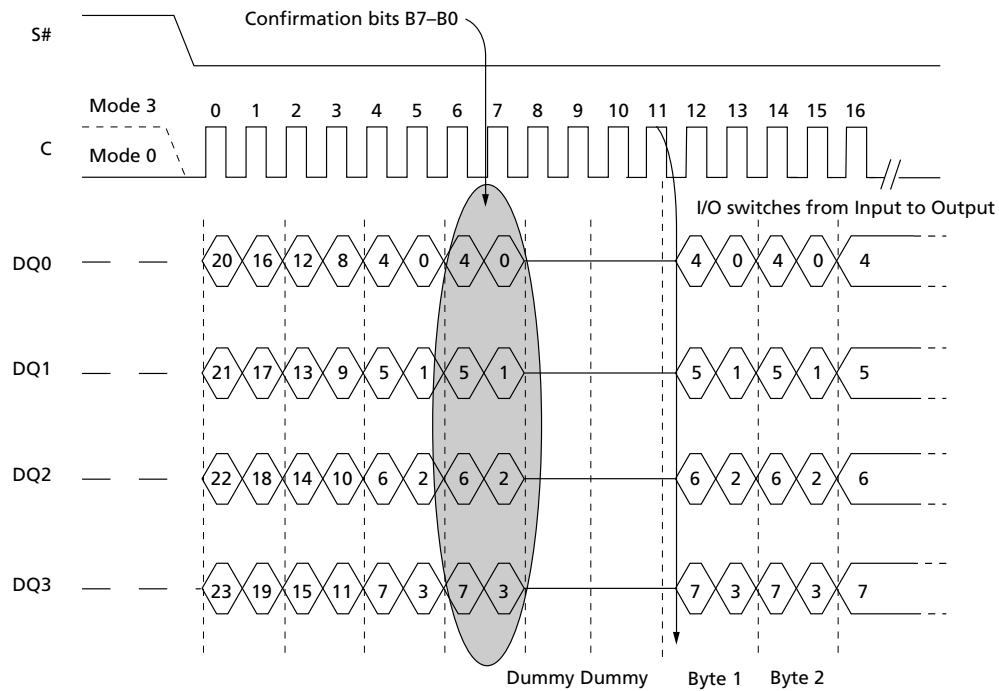


Table 5: XIP Confirmation Bit Software Commands

XIP Confirmation Bit	N25Q	MX25L
Enter/confirm XIP mode	B4 = 0 (B7 to B5 and B3 to B0 = "Don't Care")	B7 ≠ B3 and B6 ≠ B2 and B5 ≠ B1 and B4 ≠ B0
Exit XIP mode	B4 = 1 (B7 to B5 and B3 to B0 = "Don't Care")	B7 = B3 or B6 = B2 or B5 = B1 or B4 = B0



Electrical Characteristics

Table 6: DC Current Characteristics

Parameter	Symbol	N25Q		MX25L		Units
		Min	Max	Min	Max	
Standby current	I_{CC1}	–	100	–	200	μ A
Operating current (FAST READ QUAD I/O)	I_{CC3}	–	20	–	45	mA
Operating current (PAGE PROGRAM)	I_{CC4}	–	20	–	25	mA
Operating current (WRITE STATUS REGISTER)	I_{CC5}	–	20	–	40	mA
Operating current (ERASE)	I_{CC6}	–	20	–	25	mA

Table 7: DC Voltage Specifications

Parameter	Symbol	N25Q		MX25L		Units
		Min	Max	Min	Max	
Input low voltage	V_{IL}	–0.5	$0.3 V_{CC}$	–0.5	–0.8	V
Input high voltage	V_{IH}	$0.7 V_{CC}$	$V_{CC} + 0.4$	$0.7 V_{CC}$	$V_{CC} + 0.4$	V
Output low voltage	V_{OL}	–	0.4	–	0.4	V
Output high voltage	V_{OH}	$V_{CC} - 0.2$	–	$V_{CC} - 0.2$	–	V



AC Characteristics

Table 8: AC Specifications

Parameter	Symbol	Alternate Symbol	N25Q		MX25L		Units
			Min	Max	Min	Max	
Clock frequency (x1 FAST READ)	f _C	f _C	–	108	–	80	MHz
Clock frequency (x2, x4 FAST READ)	f _C	f _C	–	108	–	70	MHz
Clock frequency (READ)	f _R	f _R	–	54	–	50	MHz
S# active setup time	t ^{SLCH}	t ^{CSS}	4	–	8	–	ns
Data-in setup time	t ^{DVCH}	t ^{DSU}	2	–	2	–	ns
Data-in hold time	t ^{CHDX}	t ^{DH}	3	–	5	–	ns
S# deselect time after correct READ (ARRAY READ to ARRAY READ)	t ^{SHSL}	t ^{CSH}	20	–	15	–	ns
S# deselect time after incorrect READ or different instruction (ERASE/PROGRAM to READ)	t ^{SHSL}	t ^{CSH}	50	–	50	–	ns
Output disable time (2.7–3.6V)	t ^{SHQZ}	t ^{DIS}	–	8	–	10	ns
Clock low to output valid (30pF)	t ^{CLQV}	t ^V	–	7	–	12	ns
Output hold time	t ^{CLQX}	t ^{HO}	1	–	2	–	ns
HOLD to output Low-Z	t ^{HHQX}	t ^{LZ}	N/A	8	N/A	N/A	ns
HOLD to output High-Z	t ^{HLQZ}	t ^{HZ}	N/A	8	N/A	N/A	ns

Note: 1. AC specifications compare the fastest versions available at the full voltage range (2.7–3.6V).

Program and Erase Specifications

Table 9: Program and Erase Specifications

Operation	N25Q		MX25L25635E		Unit
	Typ	Max	Typ	Max	
PAGE PROGRAM (256 bytes)	0.5	5	1.4	5	ms
4KB SUBSECTOR ERASE	0.3	1.5	0.06	0.3	s
64KB SECTOR ERASE	0.7	3	0.7	2	s
BULK ERASE	240	480	160	400	s

Configuration and Memory Map

Table 10: Sectors and Subsectors

Sector	Subsector	Address Range	
		Start	End
511	8191	01FF F000h	01FF FFFFh
	⋮	⋮	⋮
	8176	01FF 0000h	01FF 0FFFh
⋮	⋮	⋮	⋮
255	4095	00FF F000h	00FF FFFFh
	⋮	⋮	⋮
	4080	00FF 0000h	00FF 0FFFh
⋮	⋮	⋮	⋮
127	2047	007F F000h	007F FFFFh
	⋮	⋮	⋮
	2032	007F 0000h	007F 0FFFh
⋮	⋮	⋮	⋮
63	1023	003F F000h	003F FFFFh
	⋮	⋮	⋮
	1008	003F 0000h	003F 0FFFh
⋮	⋮	⋮	⋮
0	15	0000 F000h	0000 FFFFh
	⋮	⋮	⋮
	0	0000 0000h	0000 0FFFh

Device Identification

Manufacturer identification is assigned by JEDEC. As a result, the N25Q and MX25L devices have a different manufacturer ID and memory type codes even though their memory capacity is identical. Command 9Fh is used to read these codes in both devices.

N25Q has a unique ID (UID) composed of 17 read-only bytes, which contain the following data:

- The first byte is set to 10h.
- The next two bytes of extended device ID specify device configuration (top, bottom, or uniform architecture and hold or reset functionality).
- The next 14 bytes contain optional customized factory data. The customized factory data bytes are factory programmed.

Refer to the N25Q 256Mb data sheet for more information.

Table 11: Read Identification Summary

Parameter	N25Q Code	MX25L Code
Manufacturer ID	20h	C2h
Memory type	BAh	20h
Memory capacity	19h (256Mb)	19h

Conclusion

Comparing the features of the Micron N25Q 256Mb and MX25L25635E Flash memory devices enables users to migrate applications from the MX25L25635E to the N25Q 256Mb device.



Revision History

Rev. A – 09/11

- Initial release

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