



# Technical Note

## Migrating from Atmel AT45DB011D to Micron M45PE10 Flash Devices

### Introduction

This technical note explains how to migrate to a Micron® M45PE10 from an Atmel® AT45DB011D. The discussion takes into consideration signal descriptions, packages, architectures, the software command set, performance, and block protection.

The Micron M45PE10 memory offers a standard SPI protocol. It is manufactured in 110nm technology, and provides a minimum of 100,000 PROGRAM/ERASE cycles, with data retention for 20 years.

Using the SPI standard command set, the M45PE10 can replace the competing Atmel AT45DB011D. Micron's M45PE10 offers single supply voltage ranging from 2.7V to 3.6V and is offered in the industrial temperature range (–40°C to +85°C).



## Memory Array Architecture

Table 1: Device Comparison

M45PE10 Features	AT45DB011D Features
Organization: – 2 sectors, 256 pages each; each page 256 bytes wide – Entire device is 512 pages or 131,072 bytes	Organization: – 512 pages, each 256 bytes or 264 bytes – Additional SRAM buffer of 256/264 bytes
Programming: – 1 to 256 bytes at a time	Programming: – 1 page at a time (main memory page program trough buffer)
Erase options: – 1 page at a time – 1 sector at a time	Erase options: – Page erase (256 bytes) – Block erase (one block = 2KB or 8 pages) – Sector erase (32KB per sector) <sup>1</sup> – Chip erase (1Mb)

Note: 1. Sector 0 = sector 0a (8 pages) + sector 0b (120 pages); sector 1 = 128 pages; sector 2 = 128 pages; sector 3 = 128 pages.

## Package Configurations

Table 2: Package Configurations

Package	M45PE10	AT45DB011D
SO8N (SOP2-8/150 mil)	Yes	–
VFQPN8 (6mm x 5mm MLP8) (V-PDFN-8/6mm x 5mm)	Yes	–
SO8W (SOP2-8/208 mil)	–	Yes

## Signal Descriptions

**Table 3: Signal Descriptions**

M45PE10 Signal	AT45DB011D Signal	Type	Description
C	SCK	Input	Serial clock
D	SI	Input	Serial data input
Q	SO	Output	Serial data output
S	CS	Input	Chip select
W <sup>1</sup>	WP	Input	Write protect <sup>2</sup>
RESET	RESET	Input	Reset
V <sub>CC</sub>	V <sub>CC</sub>	Power	Supply voltage
V <sub>SS</sub>	GND	Ground	Ground

- Notes: 1. The M45PE10 provides hardware protection of the bottom sector (64KB).  
2. The write protect signal ensures hardware protection in both devices.

## Commands

M45PE10 has a very simple command set, including four READ commands, two PROGRAM commands, two ERASE commands, and two deep power-down commands, with two additional commands. AT45DB011 has 30 commands used for the memory, the buffer, and for software protection.

**Table 4: Supported Command Set**

Command Name	Command Code M45PE10	Command Code AT45DB011
<b>READ</b>		
READ	03h	D2h
FAST READ	0Bh	N/A
READ STATUS REGISTER (RDSR)	05h	D7h
READ DEVICE ID (RDID)	9Fh	9Fh
CONTINUOUS ARRAY READ (legacy command)	N/A	E8h
CONTINUOUS ARRAY READ (low frequency)	N/A	03h
CONTINUOUS ARRAY READ (high frequency)	N/A	0Bh
BUFFER READ (low frequency)	N/A	D1h
BUFFER READ	N/A	D4h
READ SECTOR PROTECTION READ	N/A	32h
READ SECTOR LOCK DOWN REGISTER	N/A	35h
READ SECURITY REGISTER	N/A	77h
<b>WRITE or PROGRAM</b>		
PAGE WRITE (PW)	0Ah	N/A
PAGE PROGRAM (PP)	02h	N/A



**Table 4: Supported Command Set (Continued)**

Command Name	Command Code M45PE10	Command Code AT45DB011
BUFFER WRITE	N/A	84h
BUFFER to main memory page program with built-in erase	N/A	83h
BUFFER WRITE to main memory page program without built-in erase	N/A	83h
MAIN MEMORY PAGE PROGRAM through buffer	N/A	82h
PROGRAM SECTOR PROTECTION REGISTER	N/A	3Dh + 2Ah + 7Fh + FCh
PROGRAM SECURITY REGISTER	N/A	9Bh + 00h + 00h + 00h
AUTO PAGE REWRITE through buffer	N/A	58h
<b>ERASE</b>		
PAGE ERASE (PE)	DBh	81h
SECTOR ERASE (SE)	D8h	7Ch
BLOCK ERASE	N/A	50h
CHIP ERASE	N/A	7Ch, 94h, 80h, 9Ah
ERASE SECTOR PROTECTION REGISTER	N/A	3Dh + 2Ah + 7Fh + CFh
<b>DEEP POWER-DOWN</b>		
DEEP POWER-DOWN (DP)	B9h	B9h
RELEASE/RESUME FROM DEEP POWER-DOWN	ABh	ABh
<b>Additional Commands</b>		
WRITE ENABLE	06h	N/A
WRITE DISABLE	04h	N/A
ENABLE SECTOR PROTECTION	N/A	3Dh + 2Ah + 7Fh+ A9h
DISABLE SECTOR PROTEON	N/A	3Dh + 2Ah + 7Fh+ 9Ah
SECTOR LOCK DOWN	N/A	3Dh + 2Ah + 7Fh+ 30h
MAIN MEMORY PAGE to BUFFER TRANSFER	N/A	53h
MAIN MEMORY PAGE to BUFFER COMPARE	N/A	60h

## READ ID

**Table 5: Device ID Codes**

M45PE10			AT45DB011D		
Device ID	Memory type	40h	Device ID, part 1	Family code	001 = DataFlash
	Memory capacity	11h		Density code	00010 = 1Mb
Unique ID	CFD length	10h	Device ID, part 2	MLC code	000 = 1 bit/cell technology
	CFD content	16 bytes read-only		Product version code	00000 = initial version
Available for the T9HX processor on request		16 bytes	Extended device infor- mation string length	Byte count	00h = 0 bytes of informa- tion

Note: 1. Some bytes will be output as information data about the device if this value is anything other than 00h.



**Table 6: READ ID Command Codes**

<b>M45PE10</b>		<b>AT45DB011D</b>	
Manufacturer ID	20h	Manufacturer ID	1Fh
Memory type	40h	Device ID, part 1	22h
Memory capacity	11h	Device ID, part 2	00h
CFD length	10h	Extended device information string length	00h
CFD content	16 bytes		

## DC Specifications

**Table 7: DC Current Specifications**

Parameter	Symbol	M45PE10		AT45DB011D		Unit
		Min	Max	Min	Max	
Standby current	$I_{CC1}$	–	50	–	50	$\mu\text{A}$
Deep power-down current	$I_{CC2}$	–	10	–	25	$\mu\text{A}$
Read operating current	$I_{CC3}$	–	4 (33 MHz) 12 (75 MHz)	–	12 (33 MHz) 25 (66 MHz)	mA
Program operating current	$I_{CC4}$	–	15	–	20	mA
Erase operating current	$I_{CC5}$	–	15	–	20	mA

Note: 1. There are no significant differences in DC current specifications between the M45PE10 and AT45DB011D devices, except for the maximum value of read operating current at 33 MHz.

**Table 8: DC Voltage Specifications**

Parameter	Symbol	M45PE10		AT45DB011D		Unit
		Min	Max	Min	Max	
Input low voltage	$V_{IL}$	–0.5	$0.3V_{CC}$	–	$0.3V_{CC}$	V
Input high voltage	$V_{IH}$	$0.7V_{CC}$	$V_{CC} + 0.4$	$0.7V_{CC}$	–	V
Output low voltage	$V_{OL}$	–	0.4	–	0.4	V
Output high voltage	$V_{OH}$	$V_{CC} - 0.2$	–	$V_{CC} - 0.2$	–	V

## AC Specifications

**Table 9: AC Specifications**

Parameter	Symbol	Alternate Symbol	M45PE10		AT45DB011D		Unit
			Min	Max	Min	Max	
Clock frequency	f <sub>C</sub>	f <sub>C</sub>	–	75	–	66	MHz
Clock frequency for read (low frequency)	f <sub>R</sub>	f <sub>R</sub>	–	33	–	33	MHz
Clock high time	t <sub>CH</sub>	t <sub>WH</sub>	6	–	6.8	–	ns
Clock low time	t <sub>CL</sub>	t <sub>WL</sub>	6	–	6.8	–	ns
Chip select active setup time	t <sub>SLCH</sub>	t <sub>CSS</sub>	5	–	5	–	ns
Data-in setup time	t <sub>DVCH</sub>	t <sub>DSU</sub>	2	–	2	–	ns
Data-in hold time	t <sub>CHDX</sub>	t <sub>DH</sub>	5	–	3	–	ns
Chip select active hold time	t <sub>CHSH</sub>	t <sub>CSH</sub>	5	–	5	–	ns
Output disable time	t <sub>SHQZ</sub>	t <sub>DIS</sub>	–	8	–	6	ns
Clock low to output valid	t <sub>CLQV</sub>	t <sub>V</sub>	–	8	–	6	ns
Output hold time	t <sub>CLQX</sub>	t <sub>HO</sub>	–	0	–	0	ns

- Notes:
1. The AC specifications are similar for the M45PE10 and AT45DB011D devices at the highest operating frequency (75 MHz for the M45PE10 and 66 MHz for the AT45DB011D).
  2. See the respective device data sheets for a full listing of AC specifications. On the M45PE10 data sheet, AC specifications are also reported for operating frequencies at 25 MHz, 33 MHz, and 50 MHz.

## Program and Erase Specifications

**Table 10: Program and Erase Specifications**

M45PE10 (75 MHz Operating Frequency)				AT45DB011D				Unit
Parameter	Symbol	Typ	Max	Parameter	Symbol	Typ	Max	
PAGE WRITE cycle time (256 bytes)	$t_{PW}$	11	23	Page-to-buffer transfer time	$t_{XFR}$	–	0.4	ms
PAGE PROGRAM cycle time (256 bytes)	$t_{PP}$	0.8	3	Page programming time (256/264 bytes)	$t_P$	2	4	ms
PAGE ERASE cycle time	$t_{PE}$	10	20	PAGE ERASE time (256/264 bytes)	$t_{PE}$	13	32	ms
SECTOR ERASE cycle time (64KB)	$t_{SE}$	1500	5000	SECTOR ERASE time	$t_{SE}$	800	2500	ms
				BLOCK ERASE time (2KB)	$t_{BE}$	15	35	ms
				CHIP ERASE time	$t_{CE}$	1.8	3	s

Note: 1. The timing specifications given are related to the memory organization of the M45PE10 and AT45DB011D devices.

## Conclusion

Contrasting the key differences between Micron's M45P and Atmel's AT45DB11D NOR Flash memory devices enables users to migrate applications from the AT45D to the M45P. Contact your local representative for additional information.



## **Revision History**

### **Rev. A – 5/11**

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900  
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