



Conversion Guide (256-Mbit): Numonyx™ Embedded Flash Memory (J3 v. D, 130 nm) to Numonyx™ StrataFlash® Embedded Memory (J3-65 nm)

Application Note - 308041

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Revision History

Date of Revision	Revision	Description
December 2008	01	Initial Release.

1.0 Introduction

This document is written to assist customer conversion from Numonyx™ Embedded Flash Memory (J3 v. D) to Numonyx™ StrataFlash® Embedded Memory (J3-65 nm) on 65 nm lithography, including explanation of key hardware and software differences.

Unless otherwise indicated throughout the rest of this document, the Numonyx™ Embedded Flash Memory (J3 v. D) device is referred to as J3 v. D and the Numonyx™ StrataFlash® Embedded Memory (J3-65 nm) device is referred to as J3-65 nm.

Both J3 v. D and J3-65 nm device are offered in 32-, 64-, 128- and 256-Mbit densities. This document just covers migration from 256-Mbit J3 v. D to 256-Mbit J3-65 nm.

This document was written based on information available at the time. Any changes in specifications to the devices may not be reflected in this document. Refer to the appropriate datasheet or sales personnel for the most current information before finalizing any design.

2.0 Device Overview

The following sections provide a brief overview of the Numonyx™ Embedded Flash Memory (J3 v. D) and Numonyx™ StrataFlash® Embedded Memory (J3-65 nm) devices.

2.1 J3-65 nm

The J3-65 nm device is offered in 32-, 64-, 128- and 256-Mbit densities. This device is available in 64-Ball Easy BGA package and 56-lead TSOP packages. Its advanced features include high programming speed, enhanced security through the new password access feature, individual and instantaneous block locking and block erase/program lockout during power transitions

This document covers only the migration from 256-Mbit J3 v. D to 256-Mbit J3-65 nm. The 32-, 64- and 128-Mb densities will have a separate migration guide. These products will be SBC on 65 nm and have the target of being 100% backward compatible to the 130 nm J3 v. D.

2.2 J3 v. D

The J3 v. D device is offered in 32-, 64-, 128- and 256-Mbit densities. Its security features include OTP, Individual and Instantaneous Block Locking. This device brings reliable, low-voltage capability (3 V read, program, and erase) with high speed, low-power operation. This device is available in 64-Ball Easy BGA package and 56-lead TSOP packages.

2.3 J3 v. D vs. J3-65 nm Feature Comparison

Table 1: J3 v. D vs. J3-65 nm Comparison⁽¹⁾

Feature	J3 v. D	J3-65 nm
Density	256 Mbit	256 Mbit
V _{CC}	2.7V-3.6V	2.7V-3.6V
TSOP	Yes	Yes
Easy BGA	Yes	Yes
Initial Access Time	95 ns (256-Mbit only) 75 ns	95 ns (Easy BGA) 105 ns (TSOP)
Async Page	25 ns	25 ns
Protection Register	128 bits	128 bits
Bus width	x8/x16	x8/x16
Multiple Chip Enables	Yes (CE[2:0])	Yes (CE[2:0])
Architecture	Single bit per cell	Multi-level cell ⁽²⁾
Block Locking	Flexible block lock	Password Access Flexible block lock
Temperature	-40 °C to +85 °C	-40 °C to +85 °C
Program Suspend	Yes	Yes
Erase Suspend	Yes	Yes
ETOX™ Process	130 nm	65 nm
Write Buffer Size	16 Words	512 Words
Block Size	128 KBytes	128 KBytes
Word Program	40 μs	150 μs
Erase	1 s	0.8 s
Page Mode Reads Page Size	4 Words/8 Words	16 words
Power-up Timing	60 μs	300 μs
CFI Compatible	Yes	Yes

Notes:

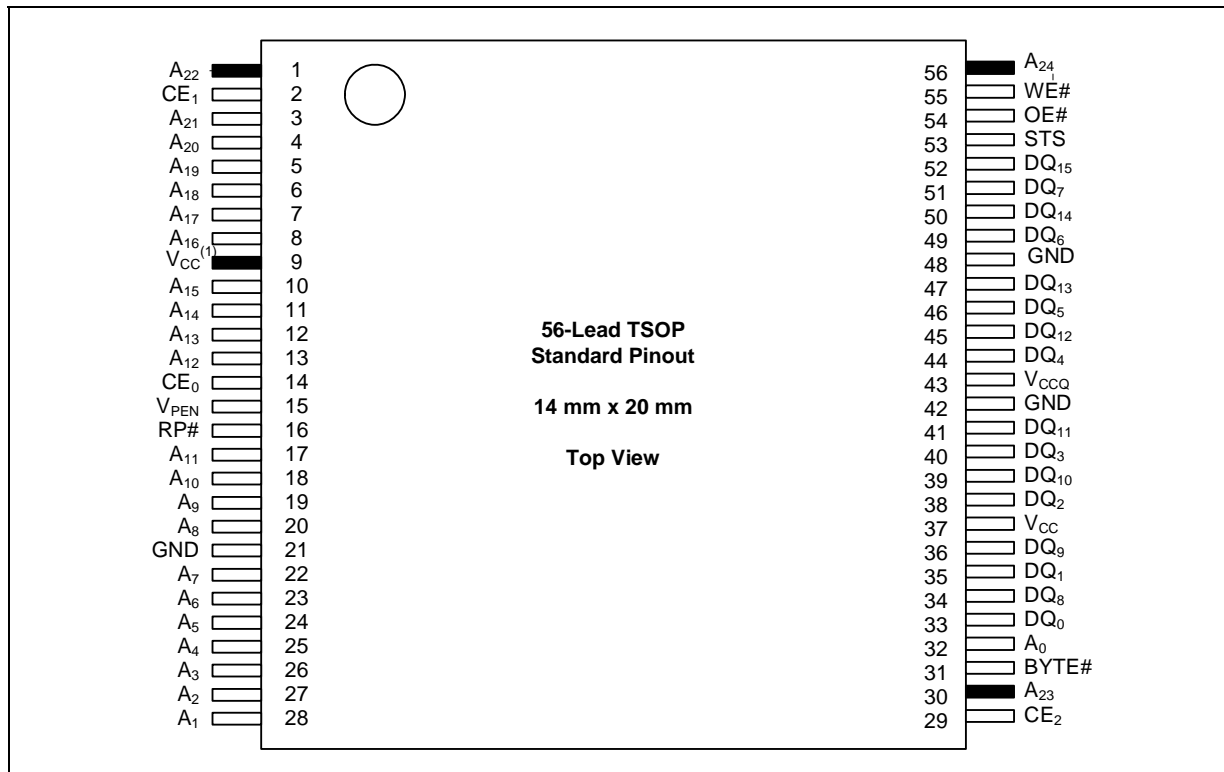
1. This table lists difference between 256-Mbit J3 v. D and 256-Mbit J3-65 nm. A separate migration guide will be available for 32-, 64- and 128-Mb devices. Target is drop in compatible with 130 nm for these densities.
2. Multi-level cell is for 256-Mbit only. 32-, 64-, 128-Mb are SBC

3.2 TSOP Pinout

The TSOP pinout is available and compatible for both J3 v. D and J3-65 nm products. The lead pitch for TSOP pinout is 0.5mm.

Pin 9 on J3 v. D is connected to Vcc. For J3-65 nm this pin has no internal connection; it may be driven or left floating.

Figure 2: 56-Lead TSOP 14 mm x 20 mm:



Notes:

1. No internal connection for pin 9; it may be driven or floated. For legacy designs, pin can be tied to V_{CC}.
2. A0 is the least significant address bit.

3.3 Signal Descriptions

Table 2: Signal Descriptions (Sheet 1 of 2)

Sym	Type	Product		Name and Function
		J3 v. D	J3-65 nm	
A0	INPUT	Yes	Yes	BYTE SELECT ADDRESS: A0 selects between high and low bytes when the device is in the x8 mode. The address is latched during a x8 program cycle. Not used in the x16 mode (i.e., the A0 input buffer is turned off when BYTE# is high).
A[max:1]	INPUT	Yes	Yes	ADDRESS INPUTS: Used for specifying the address of a location in the array. The address inputs are internally latched during Program/Erase operations. 256-Mbit: A[24:1]
DQ[7:0]	INPUT/ OUTPUT	Yes	Yes	LOW-BYTE DATA BUS: Inputs data during write cycles, Outputs data during read cycles. High-z when the chip is de-selected or the outputs are disabled. Data is internally latched during write operations.
DQ[15:8]	INPUT/ OUTPUT	Yes	Yes	HIGH-BYTE DATA BUS: Inputs data during write cycles, Outputs data during read cycles. High-z when the chip is de-selected or the outputs are disabled. Data is internally latched during write operations.
CE[2:0]	INPUT	Yes	Yes	CHIP ENABLE: Activates the 256-Mbit device control logic, decoders, and sense amplifiers. When the device is deselected, power reduces to standby levels. All the timing specifications are the same for these three signals. Device selection occurs with the last edge of CE0, CE1, or CE2 that enables the device. Device deselection occurs with the first edge of CE0, CE1 or CE2 that disables the device. For single-chip applications, CE2 and CE1 can be connected to GND
OE#	INPUT	Yes	Yes	OUTPUT ENABLE: Low, true. OE#-low enables the device's output data buffers during read cycles. OE#-high places the data outputs in High-Z and WAIT in High-Z.
WE#	INPUT	Yes	Yes	WRITE ENABLE: Low-true, WE# controls writes to the device. Address and data are latched on the rising edge of WE#.
RP#	INPUT	Yes	Yes	RESET: When low, the device is in Reset mode, which places the outputs in high-z, resets the Write State Machine, resets the device to Asynchronous Read Array mode, and minimizes current levels. RP# high enables normal operation.
STS	OPEN DRAIN OUTPUT	Yes	Yes	STATUS: Indicates the status of the internal state machine. When configured in Level mode (default mode), it acts as a Ready/Busy# signal. When configured in one of its Pulse modes, it can indicate program and/or erase completion. For alternate configurations of the STATUS ball, see the Configuration commands. STS is to be tied to V _{CCQ} with a pull-up resistor to maintain a consistent voltage when in the ready state.
BYTE#	INPUT	Yes	Yes	BYTE ENABLE: BYTE# low places the device in the x8 mode. All data is then input or output on DQ, while DQ ₈ -DQ ₁₅ float. Address A ₀ selects between high and low byte. BYTE# high places the device in the x16 mode, and turns off the Byte Select address. Address A ₁ then becomes the lowest order address.
V _{CC}	SUPPLY	Yes	Yes	DEVICE POWER SUPPLY: Core (logic) source voltage. Writes to the flash array are inhibited when V _{CC} ≤ V _{LKO} . Operations at invalid V _{CC} voltages should not be attempted.
V _{CCQ}	SUPPLY	Yes	Yes	INPUT/OUTPUT POWER SUPPLY: Output-driver source voltage. This ball can be tied directly to V _{CC} if operating within V _{CC} range.
V _{PEN}	INPUT	Yes	Yes	ERASE/PROGRAM/BLOCK LOCK ENABLE: This input controls device protection and should not be high-z. When V _{PEN} ≤ V _{PENLK} (Lockout Voltage), contents are protected against Program and Erase commands, and in case of J3, prevents the block locking.

Table 2: Signal Descriptions (Sheet 2 of 2)

Sym	Type	Product		Name and Function
		J3 v. D	J3-65 nm	
VSS/GND	POWER	Yes	Yes	GROUND: Connects device circuitry to system ground.
NC		Yes	Yes	NO CONNECT: No internal connection; can be driven or floated.
RFU		Yes	Yes	Reserved for Future Use: Retained by Numonyx for future device functionality and/or enhancement. To ensure compatibility with future devices these balls should be treated as Don't Use (DU) until further notice from Numonyx.

4.0 Hardware Design Considerations

The following section discusses hardware design considerations when converting from J3 v. D to J3-65 nm.

4.1 AC Read/Write Specs

Refer to the product datasheet for detailed list of all read timing specifications:

- Numonyx™ Embedded Flash Memory (J3 v. D) Datasheet.
- Numonyx™ StrataFlash® Embedded Memory (J3-65 nm) Datasheet.

4.2 Key AC Read Specs

Table 3: Comparison: Key AC Read Specifications

Symbol	Specification	J3 v. D	J3-65 nm
t_{AVAV}	Read Cycle time	95 ns	95 ns (Easy BGA) 105 ns (TSOP)
t_{AVQV}	Address to output delay	95 ns	95 ns (Easy BGA) 105 ns (TSOP)
t_{ELQV}	CE# low to Output Valid	95 ns	95 ns (Easy BGA) 105 ns (TSOP)
t_{EHOZ}	CEX High to Output in High Z	25 ns	20 ns

4.3 Key AC Write Specs

Table 4: Comparison: Key AC Write Specifications

Symbol	Specification	J3 v. D	J3-65 nm
t_{PHWL} (t_{PHEL})	RP# high recovery to WE#(CEX) going low.	210 ns	150 ns
t_{WP}	Write pulse width	60 ns	50 ns
t_{AVWH}	Address Setup to WE# (CEX) Going High	55 ns	50 ns
t_{WPH} t_{WHWL}	Write Pulse Width High	30 ns	20 ns
t_{WHGL}	Write Recovery before Read	35 ns	0

4.4 Program/Erase block lock specifications

Table 5: Comparison: Key Specifications (Sheet 1 of 2)

Symbol	Specification	J3 v. D	J3-65 nm
t_{VCCPH}	Vcc Power Valid to RP# de-assertion (high)	60 μ s	300 μ s
t_{WHQV3} t_{EHQV3}	Word Program (Typ)	40 μ s	150 μ s
	Word Program (Max)	175 μ s	456 μ s

Table 5: Comparison: Key Specifications (Sheet 2 of 2)

Symbol	Specification	J3 v. D	J3-65 nm
t_{WHQV4}	Block Erase Time (Typ)	1 s	0.8 s
t_{EHQV4}	Block Erase Time (Max)	4 s	4 s
t_{EHOZ}	CEx High to output in High Z	25 ns	20 ns
t_{WHRH1}	Program Suspend Latency Time to Read (Typ)	15 μ s	20 μ s
t_{EHRH1}	Program Suspend Latency Time to Read (Max)	20 μ s	25 μ s
t_{WHRH}	Erase Suspend Latency Time to Read (Typ)	15 μ s	20 μ s
t_{EHRH}	Erase Suspend Latency Time to Read (Max)	20 μ s	25 μ s
$t_{PROG/B}$	Aligned 32-word Buffered Program Time (Typ)	NA	176 μ s (typ) / 716 μ s (max)
	Aligned 64-word Buffered Program Time (typ)	NA	216 μ s (typ) / 900 μ s (max)
	Aligned 128-word Buffered Program Time (typ)	NA	272 μ s (typ) / 1140 μ s (max)
$t_{PROG/B}$	Aligned 256-word Buffered Program Time (Typ)	NA	396 μ s (typ) / 1690 μ s (max)
	Aligned 512-word Buffered Program Time (Typ)	NA	700 μ s (typ) / 3016 μ s (max)

4.5 DC Specification

The below table goes over the key differences in the DC Current and Voltage specs.

Table 6: DC Current and Voltage Specifications

Symbol	Specification	J3 v. D	J3-65 nm
I_{CCS}	V _{CC} Standby current	50 μ A (typ) / 120 μ A (max) (256M)	65 μ A (typ) / 210 μ A (max) (256M)
I_{CCR}	Page Mode Read Current	20mA ¹	16mA ²
		15mA ³	16mA ²
I_{CCW} (typ and max)	V _{CC} Program or Set Lock-Bit Current	35 mA (typ) / 60mA (max)	35 mA (typ) / 50mA (max)
I_{CCE} (typ and max)	V _{CC} Block Erase or Clear Block Lock Bits Current	35 mA (typ) / 70mA (max)	35 mA (typ) / 50mA (max)
V_{IL}	Input Low Voltage	-0.5 V (min) 0.8 V (max)	-0.5 V (min) 0.6 V (max)
V_{LKO}	V _{CC} Lockout Voltage	2.0V	1.5V
V_{LKOQ}	V _{CCQ} Lockout Voltage	NA	0.9V

1. 4-Word page read with f=5 MHz.
2. 16 Word page read with f=13 MHz.
3. 8 Word page read with f=5 MHz.

4.6 Capacitance

Table 7: Capacitance for J3-65 nm

Symbol	Parameter	J3 v. D		J3-65 nm	
		Typ	Max	Typ	Max
C_{IN}	Input Capacitance	6pF	8pF	6pF	7pF
C_{OUT}	Output Capacitance	8pF	12pF	4pF	5pF

5.0 Software Design Considerations

The following sections discuss software design considerations when converting from the J3 v. D device to the J3-65 nm device.

Table 8: J3 v. D and J3-65 nm Device Identifiers

Code Type	Device Address ⁽¹⁾	Device Type	Density	Device Identifier
Manufacturer Code	0x00	Numonyx™ Flash	All	0089
Device Code	0x01	J3-65 nm	256 Mbit	001D
		J3 v. D	256 Mbit	001D

Note: Numonyx reserves other locations within the Identifier address space for future use.

5.1 Performance Improvements in J3-65 nm

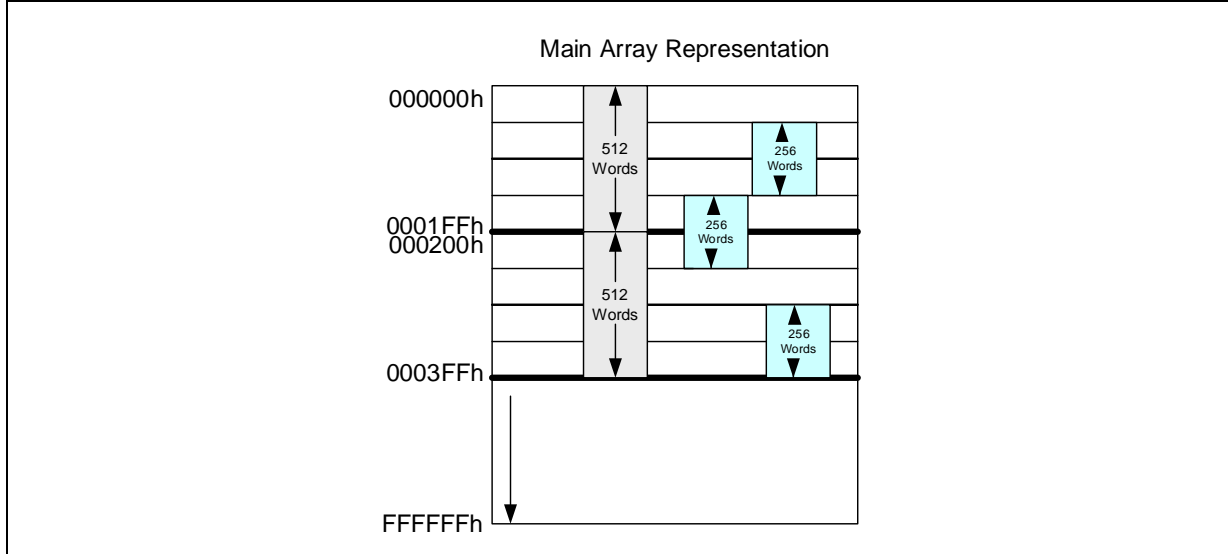
The write performance can be increased on J3-65 nm by using the 512 Word buffer. If buffered programming is being done using the 32 Byte buffer (similar to 130 nm devices), no software changes need to be implemented.

In order to achieve maximum performance using the 512 Word buffer on 65 nm devices, the following considerations apply during software modifications:

1. Use the Full 512 Word Buffer
2. If 512 Word Buffer is being used, the programming addresses should be aligned in 512 word address boundaries. For example: Start Programming address is 000000h and End Programming Address is 0001FFh. Please refer to Figure 3.
3. If the addresses must be mis-aligned, they must be in chunks of 256 Words. For example: Start Programming Address to Start Programming Address + 0000FFh (256 Words). Please refer to Figure 3.

The Read performance can be improved by providing read page buffer up to 32 Bytes (P+1Dh).

Figure 3: Main Array Representation



5.2 Password Access

Password Access is a security enhancement offered on the J3-65 nm device. This feature protects information stored in main-array memory blocks by preventing content alteration or reads, until a valid 64-bit password is received. Password Access may be combined with Non-Volatile Protection and/or Volatile Protection to create a multi-tiered solution.

Please contact your Numonyx Sales for further details concerning Password Access.

5.3 CFI Differences

During adoption of Numonyx or third party software, several differences must be taken into account. This section will describe the changes.

5.3.1 System Interface Information

The following device information can optimize system interface software. All changes between J3 v. D and J3-65 nm are noted in table below.

Table 9: System Interface Information

Offset	Length	Description	J3 v. D		J3-65 nm	
			Address	Value	Address	Value
1Fh	1	"n" such that typical single word program time-out = 2 ⁿ μ-sec	1F	64 μs	1F	256 μs
20h	1	"n" such that typical max. buffer write time-out = 2 ⁿ μ-sec.	20	128 μs	20	1024 μs
23h	1	"n" such that maximum word program time-out = 2 ⁿ times typical	23	256 μs	23	512 μs
24h	1	"n" such that maximum buffer write time-out = 2 ⁿ times typical	24	1024 μs	24	4096 μs

5.3.2 Device Geometry

This field provides critical details of flash device geometry.

Table 10: Device Geometry Definition

Offset	Length	Description	J3 v. D		J3-65 nm	
			Address	Value	Address	Value
2Ah	2	"n" such that maximum number of bytes in write buffer = 2 ⁿ	2A	32 bytes	2A	1024 bytes

5.3.3 Primary-Vendor Specific Extended Query Table

Certain flash features and commands are optional. The *Primary Vendor-Specific Extended Query* table specifies this and other similar information.

Table 11: Burst Read Information

Offset P=31h	Length	Description	J3 v. D		J3-65 nm	
			Address	Value	Address	Value
(P+13)h	1	Page Mode Read capability bits 0–7 = "n" such that 2 ⁿ HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	044	8 byte	044	32 byte

6.0 Summary

This application note enables customers to understand the hardware and software differences between the J3 v. D and J3-65 nm flash memory devices. Please refer to the relevant datasheet for additional information.

Order/Document Number	Document/Tool
316577	Numonyx™ Embedded Flash Memory (J3 v. D) Datasheet.
319942	Numonyx™ StrataFlash® Embedded Memory (J3-65 nm) Datasheet.

Note: Contact your local Numonyx or distribution sales office or visit Numonyx's World Wide Web home page at <http://www.Numonyx.com> for technical documentation, tools, and additional information.