

Conversion Guide: Numonyx™ Embedded Flash Memory J3 (128/ 128 Mbit Stacked to 256 Mbit Monolithic) 130nm to 65nm

Application Note - 308040

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Revision History

Date of Revision	Revision	Description
December 2008	01	Initial Release

1.0 Introduction

This document is written to assist customer conversion from Numonyx™ Embedded Flash Memory (J3 v. D) 128/128 Mbit stack to Numonyx™ StrataFlash® Embedded Memory (J3-65nm) 256-Mbit Monolithic version on 65nm lithography, including explanation of key hardware and software differences.

Unless otherwise indicated throughout the rest of this document, the Numonyx™ Embedded Flash Memory (J3 v. D) device is referred to as J3 v. D and the Numonyx™ StrataFlash® Embedded Memory (J3-65nm) device is referred to as J3-65nm.

Both J3 v. D and J3-65nm device are offered in 32-, 64-, 128- and 256-Mbit densities. This document just covers migration from 256-Mbit (128/128) Stacked J3 v. D to 256-Mbit Monolithic J3-65nm.

This document was written based on information available at the time. Any changes in specifications to the devices may not be reflected in this document. Refer to the appropriate datasheet or sales personnel for the most current information before finalizing any design.

2.0 Device Overview

The following sections provide a brief overview of the Numonyx™ Embedded Flash Memory (J3 v. D) and Numonyx™ StrataFlash® Embedded Memory (J3-65nm) devices.

2.1 J3-65nm

The J3-65nm device is offered in 32-, 64-, 128- and 256-Mbit densities. They are available in 64-Ball Easy BGA package and 56-lead TSOP packages. Advanced features include improved programming performance and enhanced security through the new Password Access feature. The devices are backwards compatible with the 130nm features: individual and instantaneous block locking and block erase/program lockout during power transitions.

2.2 J3 v. D

The J3 v. D device is offered in 32-, 64-, 128- and 256-Mbit densities. Its security features include OTP, Individual and Instantaneous Block Locking. This device brings reliable, low-voltage capability (3 V read, program, and erase) with high speed, low-power operation. This device is available in 64-Ball Easy BGA package and 56-lead TSOP packages.

2.3 J3 v. D Vs J3-65nm Feature Comparison

Table 1: J3 v. D vs. J3-65nm Comparison⁽¹⁾

Feature	J3 v. D 256-Mbit (128/128) Stacked	J3-65nm 256-Mbit Monolithic
Density	256 Mbit	256 Mbit
V _{CC}	2.7V-3.6V	2.7V-3.6V
TSOP	No	Yes
Easy BGA	Yes	Yes
Initial Access Time	95 ns	95 ns (Easy BGA) 105 ns (TSOP)
Async Page	25 ns	25 ns
Protection Register	128 bits	128 bits
Bus width	x8/x16	x8/x16
Multiple Chip Enables	No	Yes (CE[2:0])
Chip Enable	Yes	No
Architecture	Single bit per cell	Multi-level cell
Block Locking	Flexible block lock	Password Access Flexible block lock
Temperature	-40 °C to +85 °C	-40 °C to +85 °C
Program Suspend	Yes	Yes
Erase Suspend	Yes	Yes
ETOX™ Process	130 nm	65 nm
Write Buffer Size	32 Bytes	256 Bytes ⁽²⁾ /512 Words
Block Size	128 KBytes	128 KBytes
Word Program	40 μs	150 μs
Erase	1 s	0.8 s
Page Mode Reads Page Size	4 Words	16 words
Power-up Timing	60 μs	300 μs
Additional CFI Link ⁽³⁾	Yes	No
CFI Compatible	Yes	Yes

Notes:

1. The J3-65nm device and J3 v. D are offered in 32-, 64-, 128- and 256-Mbit densities. This table just lists difference between 256-Mbit (Stacked) J3 v. D and 256-Mbit J3-65nm.
2. For Byte mode the maximum bytes allowed is 2⁸=256 bytes.
3. Refer to [Table 14](#).

3.0 Easy BGA Mechanical Specifications

Figure 1: Easy BGA Mechanical Specifications

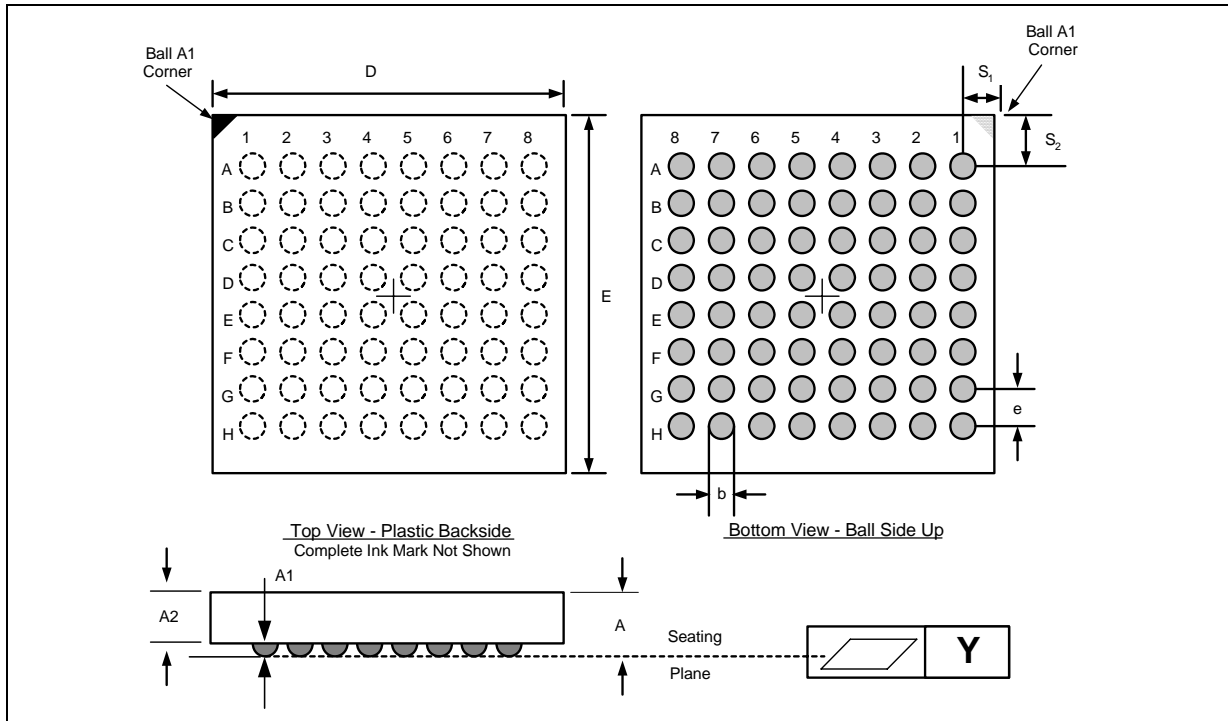


Table 2: Easy BGA Package Dimensions

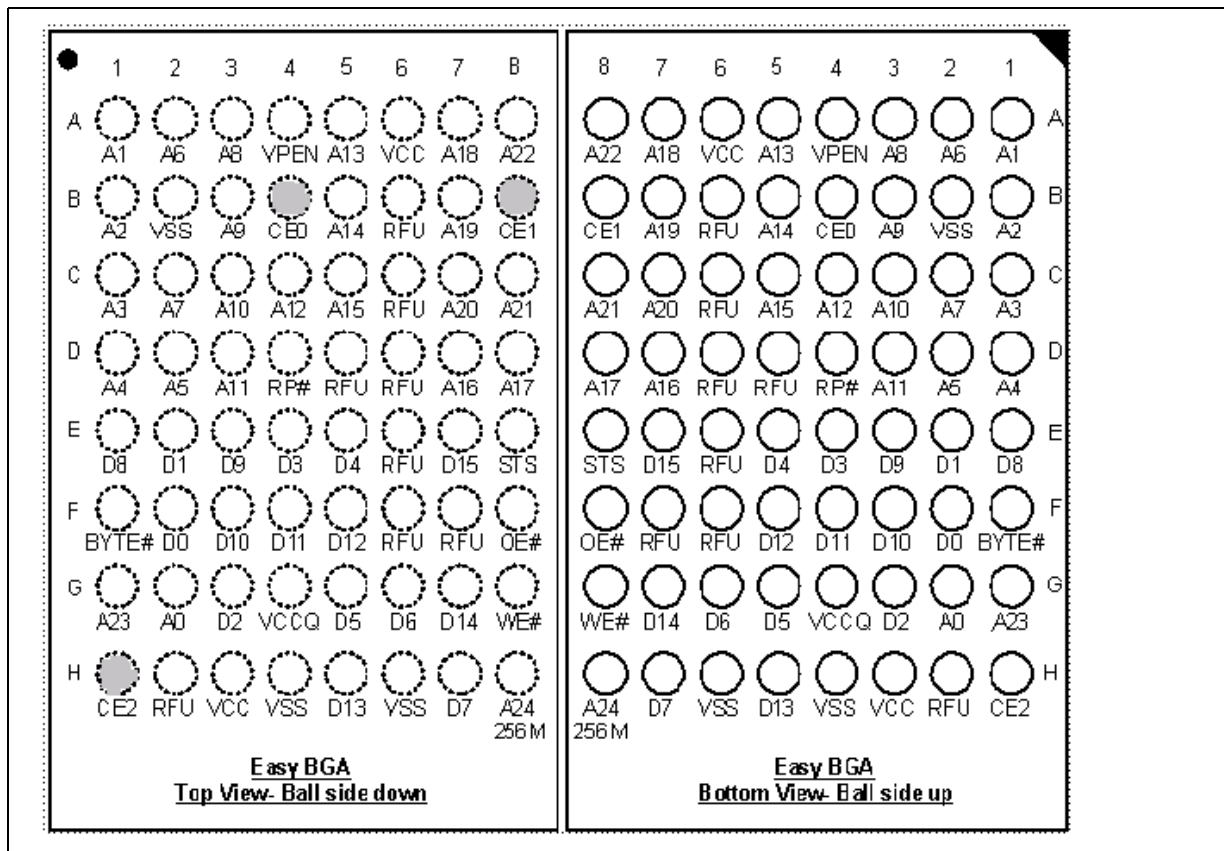
Dimension	Symbol	J3v.D 128/128 Stacked			J3-65 256 Mb Monolithic			Unit
		Min	Nom	Max	Min	Nom	Max	
Package height	A	--	--	1.300		--	1.200	mm
Ball Height	A1	0.250	--	--	0.250	--	--	mm
Package body thickness	A2	--	0.910	--	--	0.780	--	mm
Ball width	b	0.330	0.430	0.530	0.330	0.430	0.530	mm
Package body width	D	9.900	10.000	10.100	9.900	10.000	10.100	mm
Package body length	E	12.900	13.000	13.100	12.900	13.000	13.100	mm
Pitch	e	--	1.000	--	--	1.000	--	mm

4.0 Device Ballout and Signal Descriptions

4.1 Easy BGA Ballout

The Easy BGA ballout is the same for both J3 v. D and J3-65nm products. The difference is the way the Chip Enable is connected, Refer to [Table 3](#).

Figure 2: Easy BGA: 256-Mbit



Notes:

1. A0 is the least significant address bit.

Table 3: Chip Enable Connections

Signal	Ball	J3 v. D	J3-65
CE0 / CE#	B4	Connected	Connected
CE1	B8	Not Connected	Connected
CE2	H1	Not Connected	Connected

Table 4: Signal Descriptions (Sheet 1 of 2)

Sym	Type	Product		Name and Function
		J3 v. D	J3-65nm	
A0	INPUT	Yes	Yes	BYTE SELECT ADDRESS: A0 selects between high and low bytes when the device is in the x8 mode. The address is latched during a x8 program cycle. Not used in the x16 mode (i.e., the A0 input buffer is turned off when BYTE# is high).
A[max:1]	INPUT	Yes	Yes	ADDRESS INPUTS: Used for specifying the address of a location in the array. The address inputs are internally latched during Program/Erase operations. 256-Mbit: A[24:1] for Stacked devices A24 acts as a virtual CE for the two devices. A24 at VIL selects the lower die and A24 at VIH selects the upper die.
DQ[7:0]	INPUT/ OUTPUT	Yes	Yes	LOW-BYTE DATA BUS: Inputs data during write cycles, Outputs data during read cycles. High-z when the chip is de-selected or the outputs are disabled. Data is internally latched during write operations.
DQ[15:8]	INPUT/ OUTPUT	Yes	Yes	HIGH-BYTE DATA BUS: Inputs data during write cycles, Outputs data during read cycles. High-z when the chip is de-selected or the outputs are disabled. Data is internally latched during write operations.
CE[2:0]	INPUT	No	Yes	CHIP ENABLE: Activates the 256-Mbit device control logic, decoders, and sense amplifiers. When the device is deselected, power reduces to standby levels. All the timing specifications are the same for these three signals. Device selection occurs with the last edge of CE0, CE1, or CE2 that enables the device. Device deselection occurs with the first edge of CE0, CE1 or CE2 that disables the device. For single-chip applications, CE2 and CE1 can be connected to GND
CE#	INPUT	Yes	No	CHIP ENABLE: Activates the 256Mbit devices control logic, input buffers, decoders, and sense amplifiers. Device selection occurs with the first edge of CE# that enables the device. Device deselection occurs with the first edge of CE# that disables the device.
OE#	INPUT	Yes	Yes	OUTPUT ENABLE: Low-true, OE#-low enables the device's output data buffers during read cycles. OE#-high places the data outputs in High-Z.
WE#	INPUT	Yes	Yes	WRITE ENABLE: Low-true, WE# controls writes to the device. Address and data are latched on the rising edge of WE#.
RP#	INPUT	Yes	Yes	RESET: When low, the device is in Reset mode, which places the outputs in high-z, resets the Write State Machine, resets the device to Asynchronous Read Array mode, and minimizes current levels. RP# high enables normal operation.
STS	OPEN DRAIN OUTPUT	Yes	Yes	STATUS: Indicates the status of the internal state machine. When configured in Level mode (default mode), it acts as a Ready/Busy# signal. When configured in one of its Pulse modes, it can indicate program and/or erase completion. For alternate configurations of the STATUS ball, see the Configuration commands. STS is to be tied to V _{CCQ} with a pull-up resistor to maintain a consistent voltage when in the ready state.
BYTE#	INPUT	Yes	Yes	BYTE ENABLE: BYTE# low places the device in the x8 mode. All data is then input or output on DQ, while DQ ₈ -DQ ₁₅ float. Address A ₀ selects between high and low byte. BYTE# high places the device in the x16 mode, and turns off the Byte Select address. Address A ₁ then becomes the lowest order address.
V _{CC}	SUPPLY	Yes	Yes	DEVICE POWER SUPPLY: Core (logic) source voltage. Writes to the flash array are inhibited when V _{CC} ≤ V _{LKO} . Operations at invalid V _{CC} voltages should not be attempted.
V _{CCQ}	SUPPLY	Yes	Yes	INPUT/OUTPUT POWER SUPPLY: Output-driver source voltage. This ball can be tied directly to V _{CC} if operating within V _{CC} range.
V _{PEN}	INPUT	Yes	Yes	ERASE/PROGRAM/BLOCK LOCK ENABLE: This input controls device protection and should not be high-z. When V _{PEN} ≤ V _{PENLK} (Lockout Voltage), contents are protected against Program and Erase commands, and in case of J3, prevents the block locking.

Table 4: Signal Descriptions (Sheet 2 of 2)

Sym	Type	Product		Name and Function
		J3 v. D	J3-65nm	
VSS/GND	POWER	Yes	Yes	GROUND: Connects device circuitry to system ground.
NC		Yes	Yes	NO CONNECT: No internal connection; can be driven or floated.
RFU		Yes	Yes	Reserved for Future Use: Retained by Numonyx for future device functionality and/or enhancement. To ensure compatibility with future devices these balls should be treated as Don't Use (DU) until further notice from Numonyx.

5.0 Hardware Design Considerations

The following section discusses hardware design considerations when converting from J3 v. D to J3-65nm.

5.1 AC Read/Write Specs

Refer to the product datasheet for detailed list of all read timing specifications:

- Numonyx™ Embedded Flash Memory (J3 v. D) Datasheet.
- Numonyx™ StrataFlash® Embedded Memory (J3-65nm) Datasheet.

5.2 Key AC Read Specs

Table 5: Comparison: Key AC Read Specifications

Symbol	Specification	J3 v. D	J3-65nm
t_{AVAV}	Read Cycle time	95 ns	95 ns (Easy BGA) 105 ns (TSOP)
t_{AVOV}	Address to output delay	95 ns	95 ns (Easy BGA) 105 ns (TSOP)
t_{ELQV}	CE# low to Output Valid	95 ns	95 ns (Easy BGA) 105 ns (TSOP)
t_{PHQV}	RP# High to Output Delay	210 ns	150 ns
t_{EHOZ}	CEX High to Output in High Z	25 ns	20 ns

5.3 Key AC Write Specs

Table 6: Comparison: Key AC Write Specifications

Symbol	Specification	J3 v. D	J3-65nm
t_{PHWL} (t_{PHEL})	RP# high recovery to WE# (CEX) going low.	210 ns	150 ns
t_{WP}	Write pulse width	60 ns	50 ns
t_{AVWH}	Address Setup to WE# (CEX) Going High	55 ns	50 ns
t_{WPH} t_{WHWL}	Write Pulse Width High	30 ns	20 ns
t_{WHGL}	Write Recovery before Read	35 ns	0

5.4 Program/Erase block lock specifications

Table 7: Comparison: Key Specifications

Symbol	Specification	J3 v. D	J3-65nm
t_{VCCPH}	Vcc Power Valid to RP# de-assertion (high)	60 μ s	300 μ s
t_{WHQV3} t_{EHQV3}	Word Program (Typ)	40 μ s	150 μ s
	Word Program (Max)	175 μ s	456 μ s
t_{WHQV4} t_{EHQV4}	Block Erase Time (Typ)	1 s	0.8 s
	Block Erase Time (Max)	4 s	4 s
t_{EHQZ}	CEx High to output in High Z	25 ns	20 ns
t_{WHRH1} t_{EHRH1}	Program Suspend Latency Time to Read (Typ)	15 μ s	20 μ s
	Program Suspend Latency Time to Read (Max)	20 μ s	25 μ s
t_{WHRH} t_{EHRH}	Erase Suspend Latency Time to Read (Typ)	15 μ s	20 μ s
	Erase Suspend Latency Time to Read (Max)	20 μ s	25 μ s
$t_{PROG/B}$	Aligned 32-word Buffered Program Time (Typ)	NA	176 μ s (typ) / 716 μ s (max)
	Aligned 64-word Buffered Program Time (typ)	NA	216 μ s (typ) / 900 μ s (max)
	Aligned 128-word Buffered Program Time (typ)	NA	272 μ s (typ) / 1140 μ s (max)
$t_{PROG/B}$	Aligned 256-word Buffered Program Time (Typ)	NA	396 μ s (typ) / 1690 μ s (max)
	Aligned 512-word Buffered Program Time (Typ)	NA	700 μ s (typ) / 3016 μ s (max)

5.5 DC Specification

The below table goes over the key differences in the DC Current and Voltage specs.

Table 8: DC Current and Voltage Specifications

Symbol	Specification	J3 v. D	J3-65nm
I_{CCS}	V _{CC} Standby current	100 μ A (typ) / 240 μ A (max)	65 μ A (typ) / 210 μ A (max)
I_{CCR}	Page Mode Read Current	20mA ⁽¹⁾	16mA ⁽²⁾
		15mA ⁽³⁾	16mA ⁽²⁾
I_{CCW}	V _{CC} Program or Set Lock-Bit Current	35 mA (typ) / 60 mA (max)	35 mA (typ) / 50mA (max)
I_{CCE}	V _{CC} Block erase or Clear Block Lock-bits Current	35 mA (typ) / 70 mA (max)	35 mA (typ) / 50 mA (max)
V_{IL}	Input Low Voltage	-0.5 V (min) 0.8 V (max)	-0.5 V (min) 0.6 V (max)
V_{LKO}	V _{CC} Lockout Voltage	2.0 V	1.5 V
V_{LK00}	V _{CC0} Lockout Voltage	NA	0.9 V

Notes:

1. This is for 4-word page read with f=5 MHz
2. This is for 16-word page read with f=13 MHz
3. This is for 8-word page read with f=5 MHz

5.6 Capacitance

Table 9: Capacitance for J3-65nm

Symbol	Parameter	J3 v. D		J3-65nm	
		Typ	Max	Typ	Max
C_{IN}	Input Capacitance	12 pF	16 pF	6 pF	7 pF
C_{OUT}	Output Capacitance	16 pF	24 pF	4 pF	5 pF

6.0 Software Design Considerations

The following sections discuss software design considerations when converting from the J3 v. D device to the J3-65nm device.

Table 10: J3 v. D and J3-65nm Device Identifiers

Code Type	Device Address ⁽¹⁾	Device Type	Density	Device Identifier
Manufacturer Code	0x00	Numonyx Flash	All	0089
Device Code	0x01	J3-65nm	256 Mbit	001D
		J3 v. D	256 Mbit	001D

Note: Numonyx reserves other locations within the Identifier address space for future use.

6.1 Device Commands

The command set for J3 v. D and J3-65nm are compatible. For J3 v. D 128/128 Stacked version some of the commands need to be issued at the base address of the die and some commands must be repeated for each die at its base address, this need not be done for the 256-Mbit Monolithic version, please refer to the relevant datasheet for more information.

6.2 Performance Improvements in J3-65nm

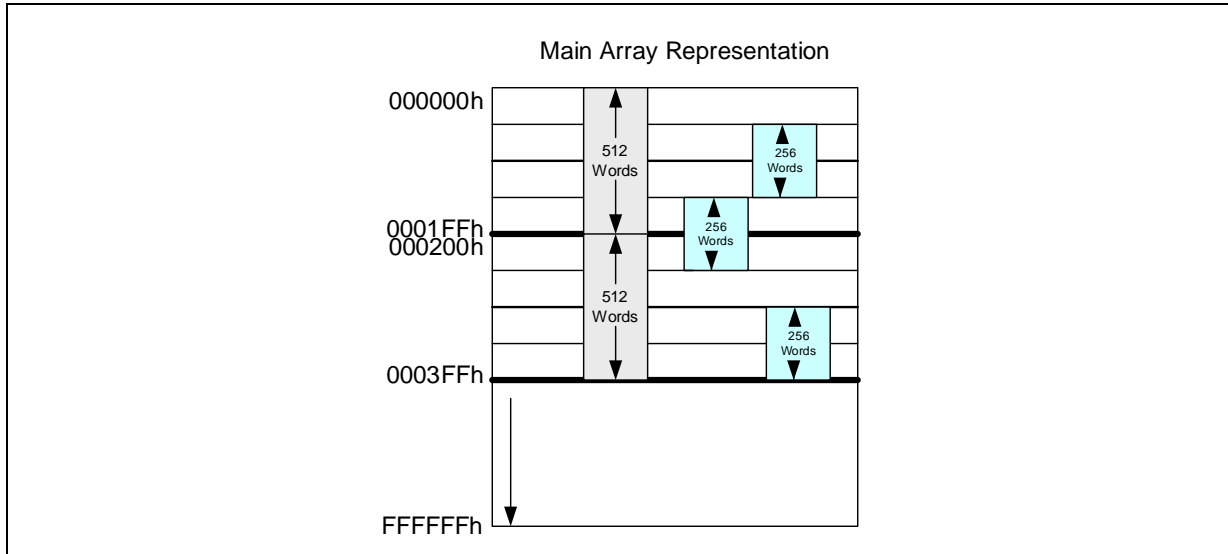
The write performance can be increased on J3-65nm by using the 512 Word buffer. If buffered programming is being done using the 32 Byte buffer (similar to 130nm devices), no software changes need to be implemented.

In order to achieve maximum performance using the 512 Word buffer on 65nm devices, the following considerations apply during software modifications:

1. Use the Full 512 Word Buffer
2. If 512 Word Buffer is being used, the programming addresses should be aligned in 512 word address boundaries. For example: Start Programming address is 000000h and End Programming Address is 0001FFh. Please refer to [Figure 3](#).
3. If the addresses must be mis-aligned, they must be in chunks of 256 Words. For example: Start Programming Address to Start Programming Address + 0000FFh (256 Words). Please refer to [Figure 3](#).

The Read performance can be improved by providing read page buffer up to 32 Bytes (P+1Dh).

Figure 3: Main Array Representation



6.3 Password Access

Password Access is a security enhancement offered on the J3-65nm device. This feature protects information stored in main-array memory blocks by preventing content alteration or reads, until a valid 64-bit password is received. Password Access may be combined with Non-Volatile Protection and/or Volatile Protection to create a multi-tiered solution.

Please contact your Numonyx Sales for further details concerning Password Access.

6.4 CFI Differences

During adoption of Numonyx or third party software, several differences must be taken into account. This section will describe the changes.

6.4.1 System Interface Information

The following device information can optimize system interface software. All changes between J3 v. D and J3-65nm are noted in table below.

Table 11: System Interface Information

Offset	Length	Description	J3 v. D		J3-65nm	
			Address	Value	Address	Value
1Fh	1	"n" such that typical single word program time-out = 2^n μ -sec	1F	64 μ s	1F	256 μ s
20h	1	"n" such that typical max. buffer write time-out = 2^n μ -sec.	20	128 μ s	20	1024 μ s
23h	1	"n" such that maximum word program time-out = 2^n times typical	23	256 μ s	23	512 μ s
24h	1	"n" such that maximum buffer write time-out = 2^n times typical	24	1024 μ s	24	4096 μ s

6.4.2 Device Geometry

This field provides critical details of flash device geometry.

Table 12: Device Geometry Definition

Offset	Length	Description	J3 v. D		J3-65nm	
			Address	Value	Address	Value
2Ah	2	"n" such that maximum number of bytes in write buffer = 2^n	2A	32 bytes	2A	1024 bytes

6.4.3 Primary-Vendor Specific Extended Query Table

Certain flash features and commands are optional. The *Primary Vendor-Specific Extended Query* table specifies this and other similar information.

Table 13: Burst Read Information

Offset P=31h	Length	Description	J3 v. D		J3-65nm	
			Address	Value	Address	Value
(P+13)h	1	Page Mode Read capability bits 0–7 = “n” such that 2n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	044	8 byte	044	32 byte

Note: This Additional CFI link shown on [Table 14](#) is not available on 256-Mbit Monolithic version

Table 14: Additional CFI Link for lower die of the stacked device.

Offset ⁽¹⁾ P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+15)h (P+16)h (P+17)h (P+18)h	4	Link Field Bit Information	46:	--10	
			47:	--10	
			48:	--00	
			49:	--00	
		Bits[9:0] = Address offset (within 32 Mbit segment) of reference CFI table	bit [9:0] = 10h	10	
Bits [27:10] = n th 32 Mbit segment of referenced CFI table	bits[27:10] = 04h	4			
Bits [30:28] = Memory type: • 000b = CSD Flash • 100b = LD Flash	bits[30:28] = 0h	0			
bit 31 = Another CFI link field immediately follows	Bit 31 = 0h	No			
(P+19)h	1	CFI Link Quantity Subfield Definition	04A	--10	
		Bits [3:0] = Quantity field (n such that n+1 equals quantity Bit 4 = Table & die relative location • 0b = Table & die on different CE# • 1b = Table & die on same CE# Bit 5 = Link field & table relative location • 0b = Table & die on different CE# • 1b = Table & die on same CE# Bits [7:6] = RFU (Set to 00b)			

7.0 Summary

This application note enables customers to understand the hardware and software differences between the J3 v. D and J3-65nm flash memory devices. Please refer to the relevant datasheet for additional information.

Order/Document Number	Document/Tool
308551	Numonyx™ Embedded Flash Memory (J3 v. D) Datasheet.
319942	Numonyx™ StrataFlash® Embedded Memory (J3-65nm) Datasheet.

Note: Contact your local Numonyx or distribution sales office or visit Numonyx's World Wide Web home page at <http://www.Numonyx.com> for technical documentation, tools, and additional information.

