AN309026
Migration Guide

How to Migrate from Numonyx M25P128 130nm to 65nm Serial Flash

This application note explains how to migrate an application based on the Numonyx™ M25P128 (130nm) to Numonyx™ M25P128 (65nm) serial flash memory device. This document does not provide detailed information on the devices, but highlights the similarities and differences between them. The comparison takes into account the signal descriptions, packages, architecture, software command set, and performance.

Introduction

The Numonyx™ M25P128 (65nm) memory offers a standard SPI protocol, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus. Manufactured on our mature 65 nm technology, this memory provides robust reliability – durability for a minimum of 10,000 program/erase cycles and data retention for 20 years. More than 500 million devices† have shipped worldwide on this technology between 2006 and the founding of Numonyx in 2008. Customers can rely on Numonyx (the merger of Intel and STMicroelectronics flash memory groups) to continue delivering highly reliable and mature products on this technology.

Using the SPI standard command set, the M25P128 (65nm) is drop in replacement for the M25P128 (130nm) serial flash device.

†Overall total including different memory densities

Contents

Memory architecture

The array architecture between M25P128 (130nm) and M25P128 (65nm) are identical.

M25P128:

a. Program 1 to 256 Bytes
b. 64 Uniform Sector Erase (2-Mbit each)
c. Bulk Erase (128-Mbit)
d. 65,536 Pages (256 bytes each)

Signals & Packaging

This section provides a detailed comparison between the 130nm and 65nm M25P128 signals and package pin-out.

Signal Description

A comparison between the 130nm and 65nm M25P128 signals is shown here.

Table 1: Signal description for the 130nm and 65nm devices

130nm Signal Name	65nm Signal Name	Description	Direction
C	C	Serial Clock	Input
D	D	Serial Data Input	Input
Q	Q	Serial Data Output	Output
$\overline{S}$	$\overline{S}$	Chip Select	Input
$\overline{HOLD}$	$\overline{HOLD}$	Hold	Input
VPP	VPP	Enhanced Program Supply Voltage or I/O	Input
V_{CC}	V_{CC}	Supply Voltage	Input
V_{SS}	V_{SS}	Ground	Input

Signal compatibility between the two devices is identical

Packages

Both the M25P128 (130nm) and M25P128 (65nm) are offered in:

1. 8×6 mm MLP8
2. SO16 (300 mil body width)

Command Set

The 130nm and 65nm M25P128 command sets are identical requires no software modification.

Table 2: Software commands for the 130nm & 65nm M25P128 devices

Commands	130nm M25P128	65nm M25P128	Comment
Write Enable (WREN)	06h	06h	Same
Write Disable (WRDI)	04h	04h	Same
Read Identification (RDID)	9Fh	9Fh	Same
Read Status Register (RDSR)	05h	05h	Same
Write Status Register (WRSR)	01h	01h	Same
READ	03h	03h	Same
FAST_READ	0Bh	0Bh	Same
Page Program (PP)	02h	02h	Same
Sector Erase (SE)	D8h	D8h	Same
Bulk Erase (BE)	C7h	C7h	Same

Read Commands

When reading the array contents, the command set for 130nm and 65nm M25P128 are identical. Both memories follow the standard 3-address byte protocol.

Program Commands

When programming the array contents, the command sets for 130nm and 65nm M25P128 are identical for page programming.

Erase Commands

When erasing the array contents, the command set for 130nm and 65nm M25P128 are identical for both sector erase and bulk erase.

Memory ID’s

Manufacturer identification is assigned by JEDEC; and thus the 130nm and 65nm M25P128 devices have the same Manufacturer ID, Memory Type codes, and Memory Capacity.

Table 3: Read Identification Summary

Codes	130nm M25P128	65nm M25P128
Manufacture ID	20h	20h
Memory Type	20h	20h
Memory Capacity	18h	18h

DC and AC Parameters

The M25P128 (130nm) and M25P128 (65nm) have nearly identical DC and AC characteristics (see below for details).

DC specifications

Table 4: DC specification differences

Parameter	Description	130nm M25P128			65nm M25P128		Unit
		Min	Max		Min	Max	
I_{CC3}	Operating Current (50MHz READ)	—	8		—	6	mA
	Operating Current (20MHz READ)	—	4		—	4	mA
V_{IH}	Input High Voltage	$0.7V_{CC}$	V_{CC}+0.2		$0.7V_{CC}$	V_{CC}+0.4	V

AC specifications

AC specification differences are shown here, comparing the full voltage range (2.7 V – 3.6 V). For the full list of AC specifications please refer to the product datasheets.

Table 5: Power-up timing specification differences

Description	Symbol	130nm M25P128		65nm M25P128		Unit
		Min	Max	Min	Max	
V_{CC} to S low	t_{VSL}	60	—	200	—	µs
Time delay to write instruction	t_{PUW}	1,000	10,000	400	—	µs

Table 6: AC specification differences

Description	Symbol	130nm M25P128			65nm M25P128			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Frequency (FAST READ)	f_C	—	—	50	—	—	54	MHz
Clock Frequency (READ)	f_R	—	—	20	—	—	33	MHz
S active setup time (relative to C)	t_{SLCH}	5	—	—	4	—	—	ns
S not active hold time (relative to C)	t_{CHSL}	5	—	—	4	—	—	ns
Data in hold time	t_{CHDX}	5	—	—	3	—	—	ns
S active hold time (relative to C)	t_{CHSH}	5	—	—	4	—	—	ns
S not active hold time (relative to C)	t_{SHCH}	5	—	—	4	—	—	ns
S deselect time	t_{SHSL}	100	—	—	50	—	—	ns
Clock low to output valid (30 pF)	t_{CLQV}	—	—	8	—	—	8	ns
Output hold time	t_{CLQX}	0	—	—	1	—	—	ns
HOLD setup time (relative to C)	t_{HLCH}	5	—	—	4	—	—	ns
HOLD hold time (relative to C)	t_{CHHH}	5	—	—	4	—	—	ns
HOLD setup time (relative to C)	t_{HHCH}	5	—	—	4	—	—	ns
HOLD hold time (relative to C)	t_{CHHL}	5	—	—	4	—	—	ns
Write status register cycle time	t_W	—	5	15	—	1.3	15	s

Program & Erase Times

Key program and erase time differences are shown below. For a detailed list of all parameters refer to the product datasheets.

Table 7: AC specification differences

Description	Symbol	130nm M25P128				65nm M25P128			Unit
		Min	Typ	Max		Min	Typ	Max	
Page Program cycle time (256 Bytes)	t_{PP}	—	2.5	7		—	0.5	5	ms
Page Program cycle type (n Btyes)		—	2.5			—	Int(n/8) x 0.015		
Page Program cycle time (V_{PP}=V_{PPH} @ 256 Bytes)		—	1.2			—	0.4		
Sector Erase cycle time	t_{SE}	—	2	6		—	1.6	3	s
Sector Erase cycle time (V_{PP} = V_{PPH})		—	1.6			—	1.6		
Bulk Erase cycle time	t_{BE}	—	105	250		—	130	250	s
Bulk Erase cycle time (V_{PP} = V_{PPH})		—	55			—	120		

Revision history

Table 8. Document revision history

Date	Revision	Changes
November 2009	1	Initial release

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