Migration Guide for Numonyx StrataFlash® Cellular Memory (M18), 90 nm to 65 nm

Application Note - 860

November 2007

Order Number: 315651-02

Contents

Revision History

Date	Revision	Description
October 2006	001	Initial public release
November 2007	02	Applied Numonyx branding.

1.0 Introduction

This application note describes technical requirements to migrate from the Numonyx™ StrataFlash® Cellular Memory (M18), 512 Mbit 90 nm device to the Numonyx StrataFlash® Cellular Memory (M18), 1 Gbit 65 nm device. This application note also highlights the key differences and similarities between the 512 Mbit and 1 Gbit devices.

Note: For the sake of brevity, throughout the rest of this document, the Numonyx StrataFlash® Cellular Memory (M18), 512 Mbit 90 nm device is referred to as the 512 Mbit M18 90 nm device and the Numonyx StrataFlash® Cellular Memory (M18), 1 Gbit 65 nm is referred as the 1 Gbit M18 65 nm device.

This document was written based on device information available at the time. Any changes in specifications to either device might not be reflected in this document. Refer to the appropriate documents or sales personnel for the current product information before finalizing any design.

2.0 Features Comparison

The 512 Mbit M18 90nm device and the 1 Gbit M18 65 nm device have the same product features. However, some of the electrical specifications vary slightly between the two lithographies. There are some notable differences between the two devices. The first is the 65nm product has an improved programming performance. Some other differences are the standby current and device ID's are not the same, as these deltas are driven by the fact that the 65 nm product is 1 Gbit monolithic die. In addition the buffered program partition status for the 90nm part is different than the 65nm product, and the details around these difference s are documented in Application Note 816. Table 1 below outlines various features and specifications of each device.

Note: The 1 Gbit M18 65 nm device has the same form, fit, and function as the 512 Mbit M18 device.

Table 1: Device Comparison (Sheet 1 of 2)

Feature		Specification	
		512 Mbit M18, 90 nm device	**1 Gbit M18, 65 nm device**
Device Density	512-Mbit	Yes	No
	1.0-Gbit	No	Yes
Temperature	Operating Temperature	–30°C to +85°C	
Partition Architecture	Block Structure	Symmetrical (8 Partitions)	
	Partition Layout	8 x 64Mbit	8 x 128Mbit
Operating Voltage Range	V_{CC} (core)	1.7V to 2.0V	
	V_{CCQ} (I/O)		
Performance	Asynch. Initial Access (t_{AVQV})	96 ns	
	Asynch, Page Access (t_{APA})	15 ns	
	Synch. Burst Read (t_{CHQV})	7ns @ 108MHz	
	V_{CC} Standby Current (Typ/Max)	50/120 µA	70/185 µA
Security	Flexible Block Locking	Yes	
	OTP Space	128 bits + 2k bits	

Table 1: Device Comparison (Sheet 2 of 2)

Feature		Specification	
		512 Mbit M18, 90 nm device	1 Gbit M18, 65 nm device
Program/Erase	Program Time 512 Words ($t_{PROG/PB}$)	2.15 ms (475 kB/s)	1.64 ms (650 kB/s)
	Buffered Enhanced Factory Program	Yes	
	Cycles	100,000	
Buffered Programing (BP)	Read Mode Post BP Setup (0xE9) / Read Mode Post BP Confirm (0xD0) *	Switches to Read Status Mode / Read Status Mode	Stays in Previous Read Mode / Read Status Mode
	BP Confirm Command (0xD0) Issued to Different Block Address	Buffer Program Will Not Abort	Buffer Program Will Abort & Set Error Status Bits 4 & 5
I/O Bus	Bus Width	x16	
Device ID	Non-Mux	887E	88B0
	A/D-Mux	8881	88B1

Note: * Details regarding Buffered Program Partition Status can be found in Application Note 816 "Effect of Program Buffer Size On System Interrupt Latency"

3.0 Package and Ballouts

The 1 Gbit M18, 65 nm device is available in three different package types (x16C/ x16D/x16SB). These packages will provides socket compatibility with some of the 512 Mbit M18, 90 nm device. The package height for the 65 nm line items is thinner due to the fact that the 1.0Gbit device is monolithic. Table 2 summarizes the different 90nm line items and their 65nm conversion equivalent.

Table 2: Package Size Comparison

Flash Density	Ram Density	Ball Type	512 Mbit M18, 90 nm device		1 Gbit M18, 65 nm device	
			Size (mm)	Ordering Information	Size (mm)	Ordering Information
1.0 Gbit	N/A	x16D	8x10x1.4	PF48F5500M0Y0B0	8x10x1.0	PF48F6000M0Y0BE
1.0 Gbit	256 Mbit PSRAM	x16C	8x11x1.4	PF38F5566MMYC0	11x11x1.2	PF38F6070M0YCE
1.0 Gbit	256 Mbit SRDRAM	x16D	9x11x1.4	PF38F5570MMYB0	9x11x1.2	PF38F6070M0YBE

3.1 x16D (105-Ball) Ballout, Non-Mux

Figure 1: x16D (105-Ball) Electrical Ballout, Non-Mux

Pin 1

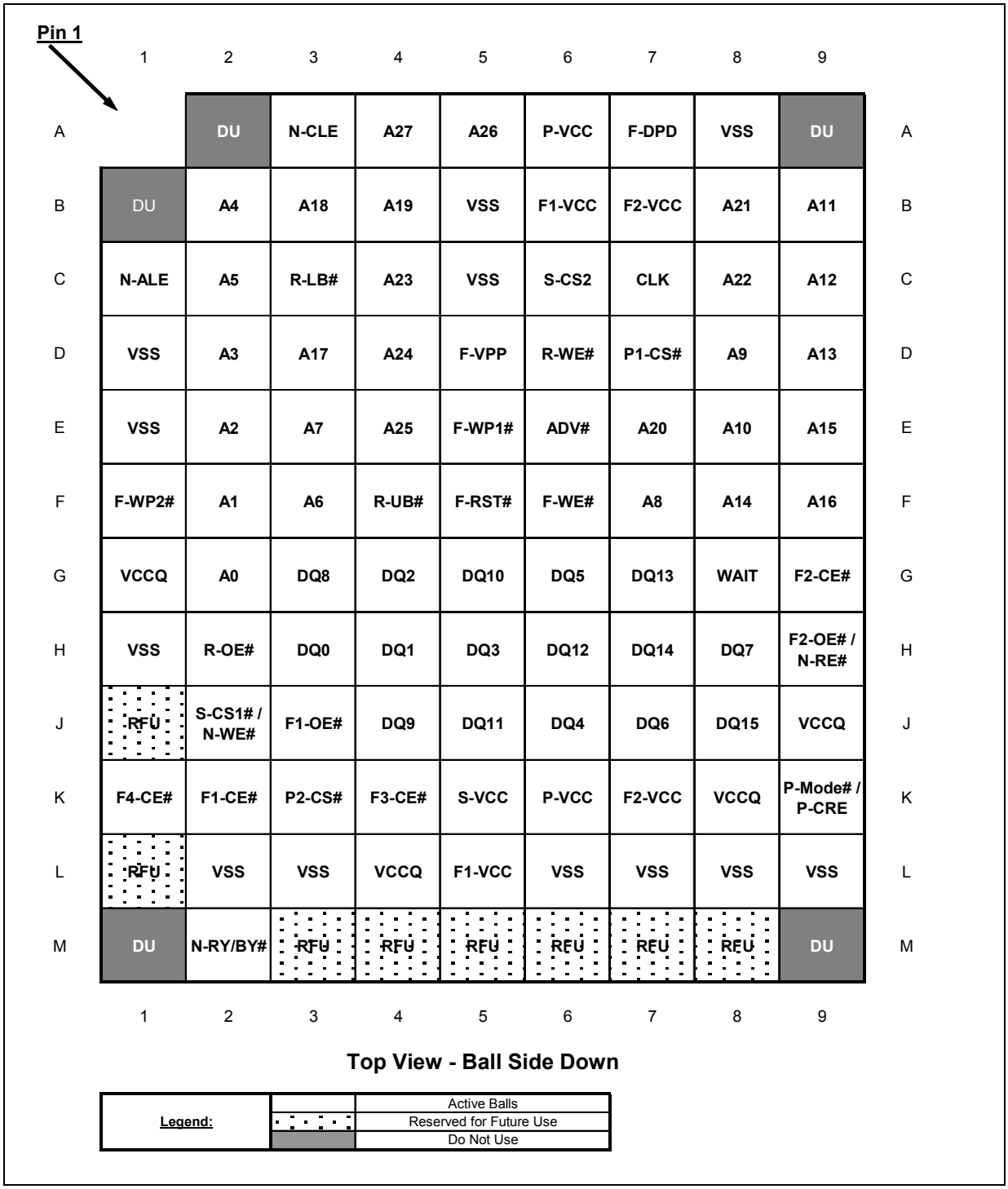
	1	2	3	4	5	6	7	8	9	
A	DU	A4	A6	A7	A19	A23	A24	A25	DU	A
B	A2	A3	A5	A17	A18	F-DPD	A22	A26	A16	B
C	A1	VSS	VSS	VSS	D-VCC	VSS	VSS	VSS	A15	C
D	A0	S-VCC	D-VCC	F1-VCC	ADV#	F2-VCC	D-VCC	N-ALE	A14	D
E	F-WP1#	WE#	D2-CS#	Depop (Index)	N-CLE	F4-CE# / A27	A21	A10	A13	E
F	F-WP2#	D1-CS#	D-CAS#	D-RAS#	Depop (RFUs)	N-RE# / S-CS1#	A20	A9	A12	F
G	RFU	F2-CE#	F1-CE#	D-BA0	Depop (RFUs)	D-CKE	F-RST#	A8	A11	G
H	N-RY/BY#	N-WE# / S-CS2	F3-CE#	D-BA1	D-CLK#	D-WE#	OE#	D-DM1 / S-UB#	D-DM0 / S-LB#	H
J	F-VPP	VCCQ	VCCQ	F1-VCC	D-CLK	F2-VCC	VCCQ	VCCQ	F-WAIT	J
K	DQ2	VSS	VSS	VSS	F-CLK	VSS	VSS	VSS	DQ13	K
L	DQ1	DQ3	DQ5	DQ6	DQ7	DQ9	DQ11	DQ12	DQ14	L
M	DU	DQ0	D-LDQS	DQ4	DQ8	DQ10	D-UDQS	DQ15	DU	M
	1	2	3	4	5	6	7	8	9	

Top View - Ball Side Down

Legend:		
		Active Balls
		De-Populated Balls
		Reserved for Future Use
		Do Not Use

3.2 x16C (107-Ball) Ballout, Non-Mux

Figure 2: x16C (107-Ball) Electrical Ballout, Non-Mux



3.3 x16 Split Bus(165-Ball) Ballout

Figure 3: x16 SPlit Bus (165 Active Ball) Electrical Ballout