

# Technical Note

## Designing for 1.5V, Low-Power FBDIMMs

### Introduction

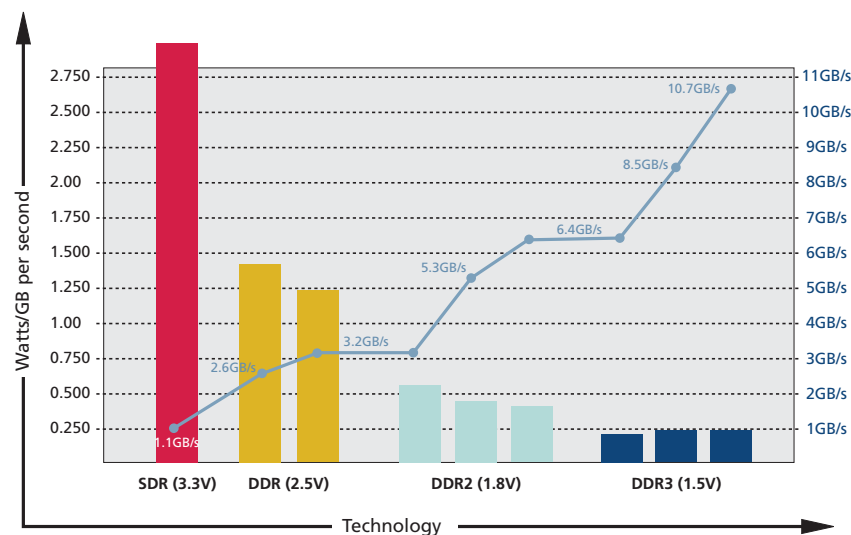
Today's memory power usage may have an adverse effect on the overall system level power and server cooling requirements. This document discusses memory power trends, identifies new, low-voltage (lower-power) solutions for high-density DDR2 memory designs, and provides details for software and hardware implementation.

### Where Does the Memory Power Come From?

Memory has migrated from simple synchronous devices to very complex, digital-state machines. Even the typical data sheet of today's high-speed memory trumps the size of the early microprocessor data sheets. Given the complex systems, it's no wonder more power is consumed in today's high-density memory modules.

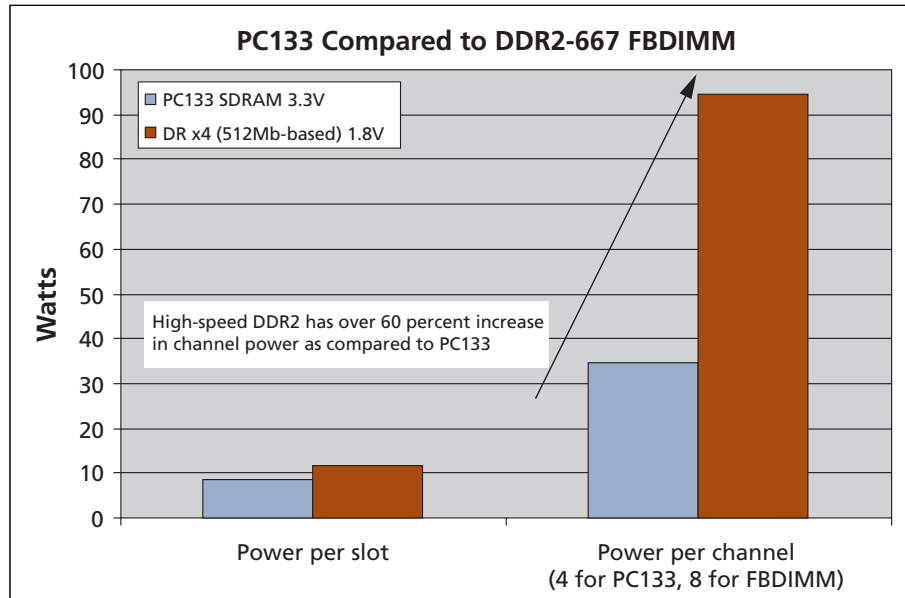
Even with the new technology, though, we've seen great improvements in the power management of memory since the early days of fast-page DRAM. As shown in Figure 1, you can see how the power per bandwidth significantly decreases with the each new technology. Early SDR-133 ran at a peak bandwidth of 1.1 GB/s for a 64-bit data bus, yet it consumed well over 400mW per active device. In comparison, DDR3-1333 provides a bandwidth for a 64-bit bus of up to 10.7 GB/s but consumes about only 300mW per device. This equates to over a 90% savings in terms of W/GB/s (SDR-133 = 3.1 W/GB/s; DDR3-1333 = 230 mW/GB/s).

**Figure 1: Industry Power Trends for Memory**



power per-bandwidth values, the actual system-level power—due to a high memory count and extremely fast cycle times—continues to grow. It's not uncommon for a dual-channel system, fully populated with eight FBDIMMs, to consume power in excess of 60–90 watts (see Figure 2).

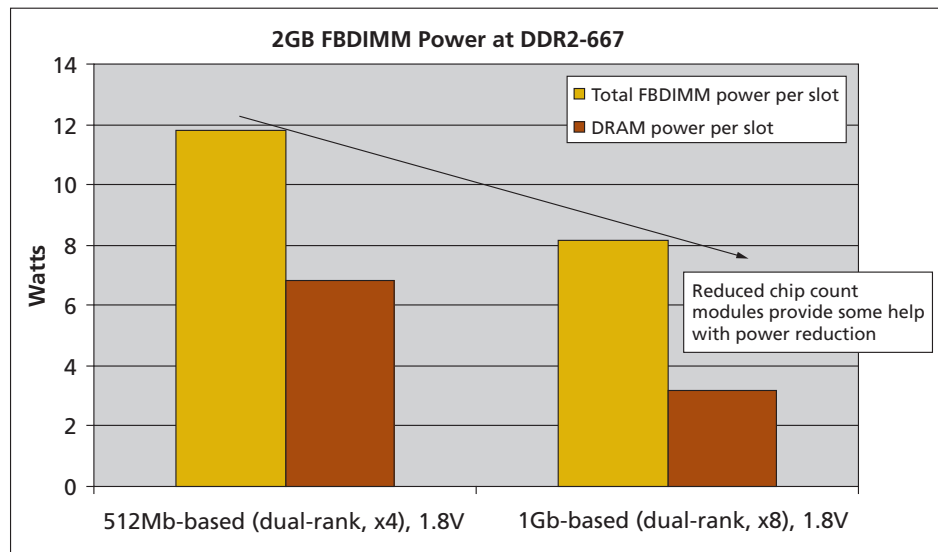
**Figure 2: Power of a Fully Loaded FBDIMM Channel**



and actual usage conditions of the DRAM is probably one of the most important factors: the faster the clock, the faster the data rate, the higher the power use. Other factors include whether or not open pages are utilized, the use of special power-down and standby modes—which are initiated with clock enable (CKE), how many slots are populated, and the module configuration types.

For example, a 2GB FBDIMM can be built at least two ways and each results in different power consumption. One method uses 512Mb (128 Meg x 4) devices; another uses 1Gb (128 Meg x 8) devices. The 512Mb-based module requires 36 DRAM, making it a dual-rank, x4 module. By contrast, the 1Gb-based module only requires 18 DRAM, making it a dual-rank, x8 module. The 1Gb-based module provides the same density at the same speed, but reduces individual module power by approximately 30% (see Figure 3 on page 3).

**Figure 3: Comparison of 2GB FBDIMM: 512Mb-Based (Dual-Rank, x4) to 1Gb-Based (Dual-Rank, x8)**



loaded (1.8V) FBDIMM channel can still consume a large amount of power. This becomes especially important when we look at a typical data center that may host rows of server racks with hundreds of FBDIMM modules, all operating simultaneously. This model could equate to kilowatts just for memory. This is why Micron developed a line of low-voltage, low-power, 1.5V DDR2 and LV FBDIMMs.

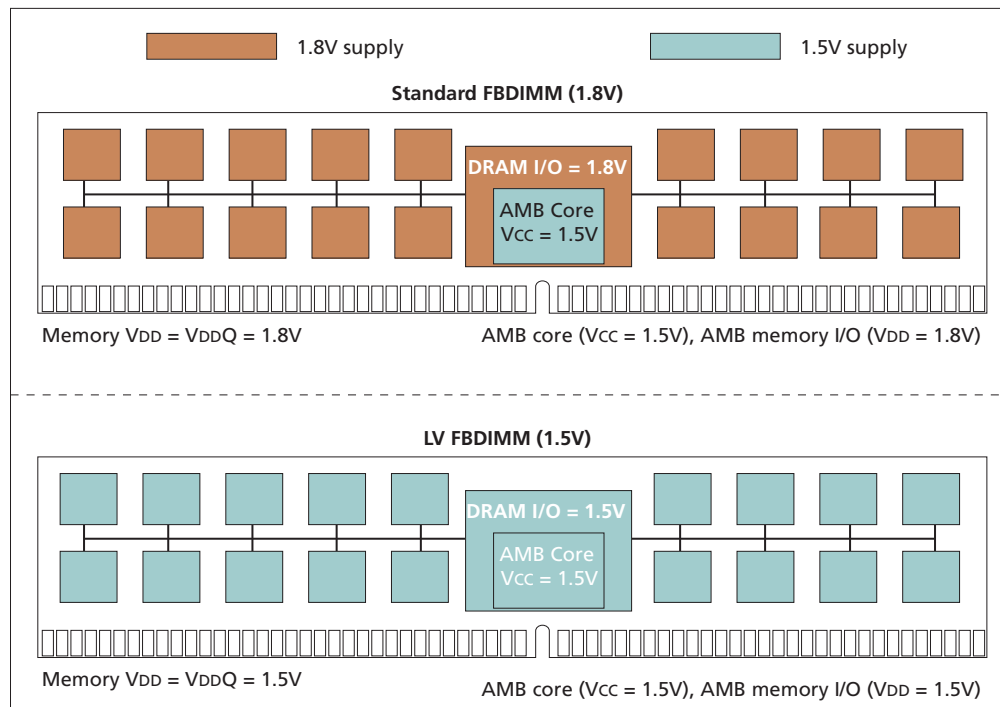
## What is an LV FBDIMM?

As the development leader of low-voltage DDR2 memory, Micron worked closely with JEDEC and many of the advanced memory buffer (AMB) vendors to ensure that the key AMB suppliers can support low-voltage DDR2 SDRAM. In addition, several of the major AMB suppliers are starting to release reduced-power AMBs that can be utilized with reduced-voltage DDR2 memory.

The result of this effort is our LV FBDIMM (low-voltage, fully buffered, dual, in-line memory module) that runs from a true 1.5V supply rail and has a substantially lower operating power than has ever been possible with conventional 1.8V DDR2 memory. The original FBDIMM required a full 1.8V supplied to the DDR2 memory and an additional 1.5V supplied to the AMB.

What's even more amazing is that, other than the voltage change, the use of LV FBDIMMs is invisible to the system. The high-speed northbound and southbound links between the memory controller and the FBDIMM modules populated in the channel are exactly the same—they already run at 1.5V. The performance, timing, and other operating requirements for the LV FBDIMM are identical to the 1.8V FBDIMM; it just consumes considerably less power (see Figure 4 on page 4).

**Figure 4: LV FBDIMM Block Diagram**

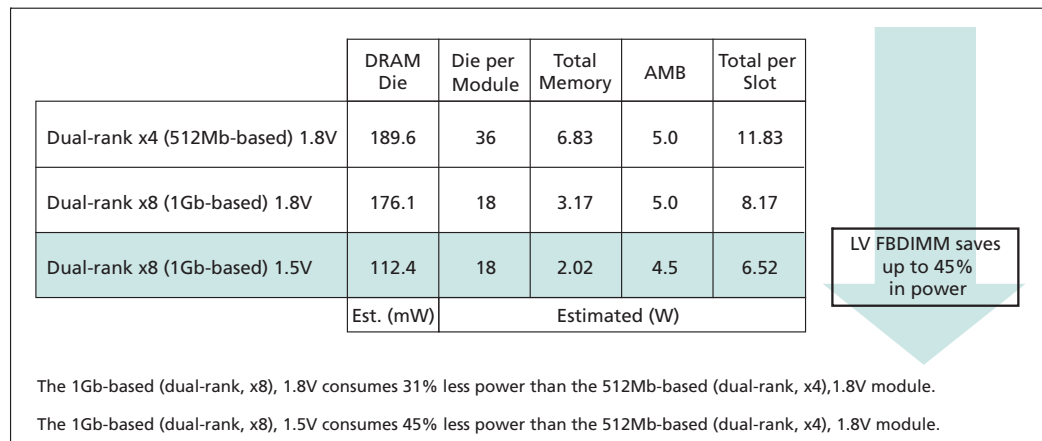


## Power Advantages of Micron's LV FBDIMMs

where  $\text{Power} = \text{Voltage} \times \text{Current}$ . The power savings from  $P = VI$  for operating DDR2 at 1.5V rather than 1.8V is about 16%.

Our LV DDR2 (1.5V) has additional power savings, too, since it is designed and manufactured on our DDR3 process, which is a true 1.5V process. This process enables us to bypass the voltage regulator—which is not very efficient—and, as such, the unregulated 1.5V DDR2 memory reduces power by an additional 15–20%. An example of power savings for a 2GB LV FBDIMM (dual-rank, x8) as compared to 2GB FBDIMM 1.8V (dual-rank, x8 and dual-rank, x4) is in the 30–45% range, respectively.

**Figure 5: Micron's LV FBDIMM Offers Up to 45% Power Savings**



[micron.com/powercalc](http://micron.com/powercalc). It's easy to estimate accurately the amount of power savings for a DRAM by loading the power calculator with the 1.5V device IDD values and then changing both the test and operating voltage from 1.8V to 1.5V.

### Other Advantages of Micron's LV FBDIMMs

available. However, if these same systems supported LV FBDIMM, the savings from the 1.5V memory could enable the systems to be fully populated and to utilize x4-based, higher-density modules or higher-speed memory—which could extend the life of an otherwise marginally obsolete system.

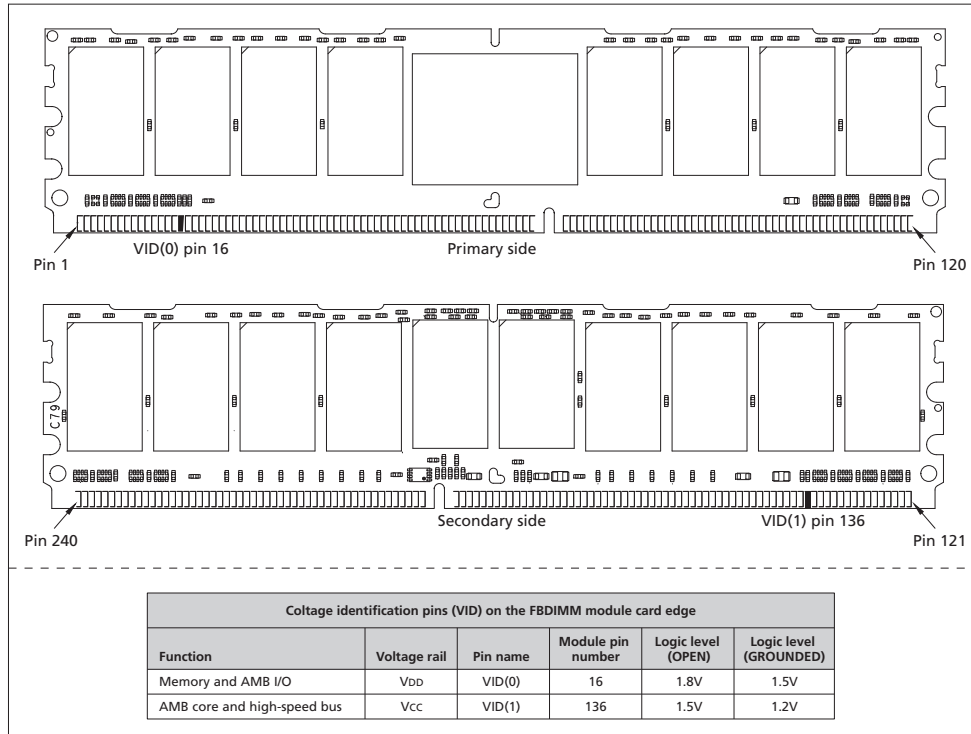
### System-Level Options with LV FBDIMMs

rather than at  $V_{DDQ} = 1.8V$ . This interface works identical to the 1.8V interface with the exception of changes to input/output voltage levels. Again, timing, speed, and general performance of the DRAM, AMB, or FBDIMM are not affected. Of course, to take advantage of the LV FBDIMM features, the system must use 1.5V DRAM and an AMB that is designed to interface with the 1.5V DRAM.

Q = 1.5V

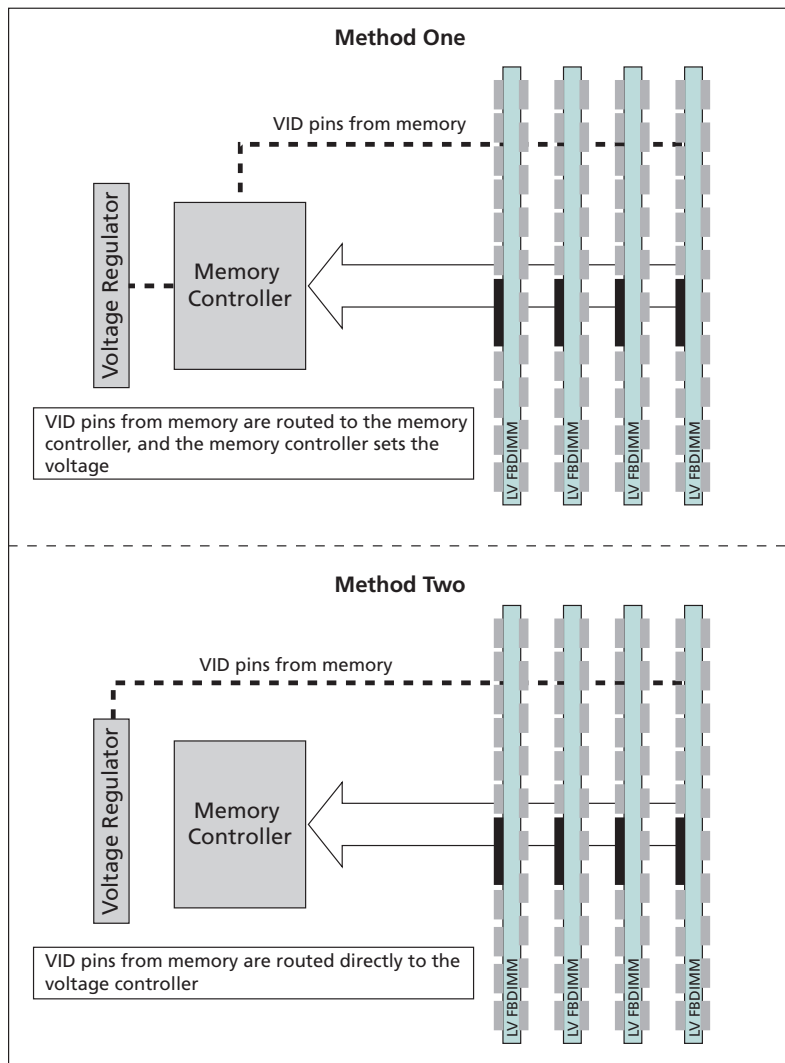
### Preparing to Design in LV FBDIMMs

**Figure 6: Using Module VID Pins for Voltage Detection**



## Implementation of the VID Pins

**Figure 7: Using Module VID Pins for Voltage Detection**



- 1.8V memory only
- 1.5V memory only
- An intermediate voltage of 1.55V, which also must be backward-compatible with the 1.8V memory

Byte 3 works like the VID pins because it flags different voltage options for the AMB core. Some AMB vendors may support a lower AMB core voltage. Under normal conditions and for most AMBs, this voltage is always set to 1.5V.

CC = 1.5V for the AMB core and VDD = 1.8V for the memory, byte 3 is programmed as 12 hex. If the module supports VCC = 1.5V for the AMB core and VDD = 1.5V for the memory, byte 3 will be programmed as 22 hex. See Figure 8 for more detail on the decoding of each bit.

SPD Byte 3	
Bit 7–Bit 4	Bit 3–Bit 0
VDD (memory voltage)	VCC (AMB voltage)
0001 = 1.8V	0001 = 1.8V
0010 = 1.5V	0010 = 1.5V
0011 = 1.2V	0011 = 1.2V
0100 = 1.55V (TBD)	All others reserved
All others reserved	

**For LV FBDIMM with standard voltage AMB,  
byte 3 equals 22 hex**

For a platform that supports dual voltages and uses the SPD to detect the memory voltage, the system must read the status of byte 3 and then condition the power as required. There are three ways to accomplish this:

1. The system can power up only the SMBus without providing a power source to the memory, read the status of byte 3, then configure the power for either the standard memory voltage level or the optional, low-voltage level of 1.5V. The system can then power-up the complete FBDIMM with the correct memory voltage, as determined by the contents of byte 3 in the SPD.
2. A second method is to power up the complete FBDIMM module with the memory voltage set to the standard voltage level of 1.8V. As part of the normal sequence, the system will read the contents of the SPD and configure the memory timing, loading, and other as required. If the system detects that byte 3 has been set for the reduced voltage level, the system will reset and cycle the memory voltage to 1.5V and restart the initialization sequence.
3. The third method is to power up the complete FBDIMM with the memory voltage set to 1.5V, read the SPD data, and then reset the voltage to 1.8V, if indicated by byte 3 in the SPD. These methods and flows are clearly identified in the following charts.

**Figure 9: Flowchart for First Power Up of System (VDD = 1.5V or 1.8V)**

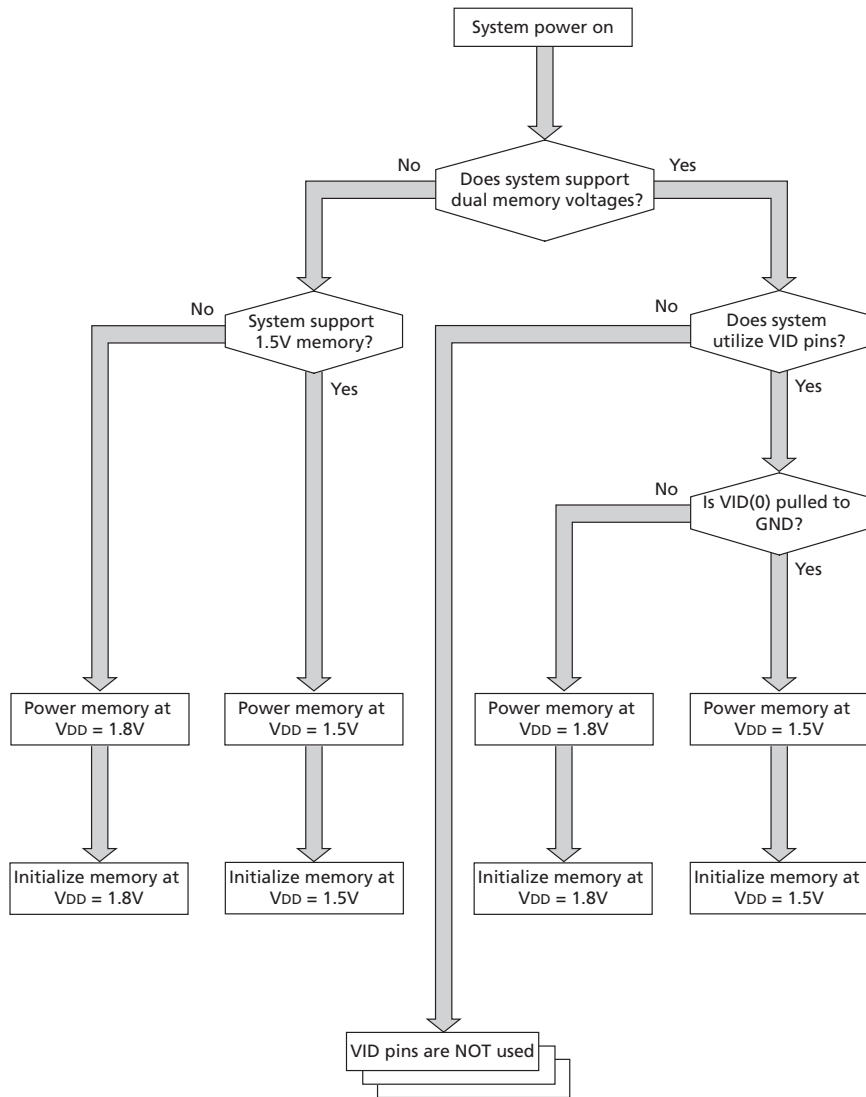


Figure 10: Reading SPD Data (VID Pins not Used)

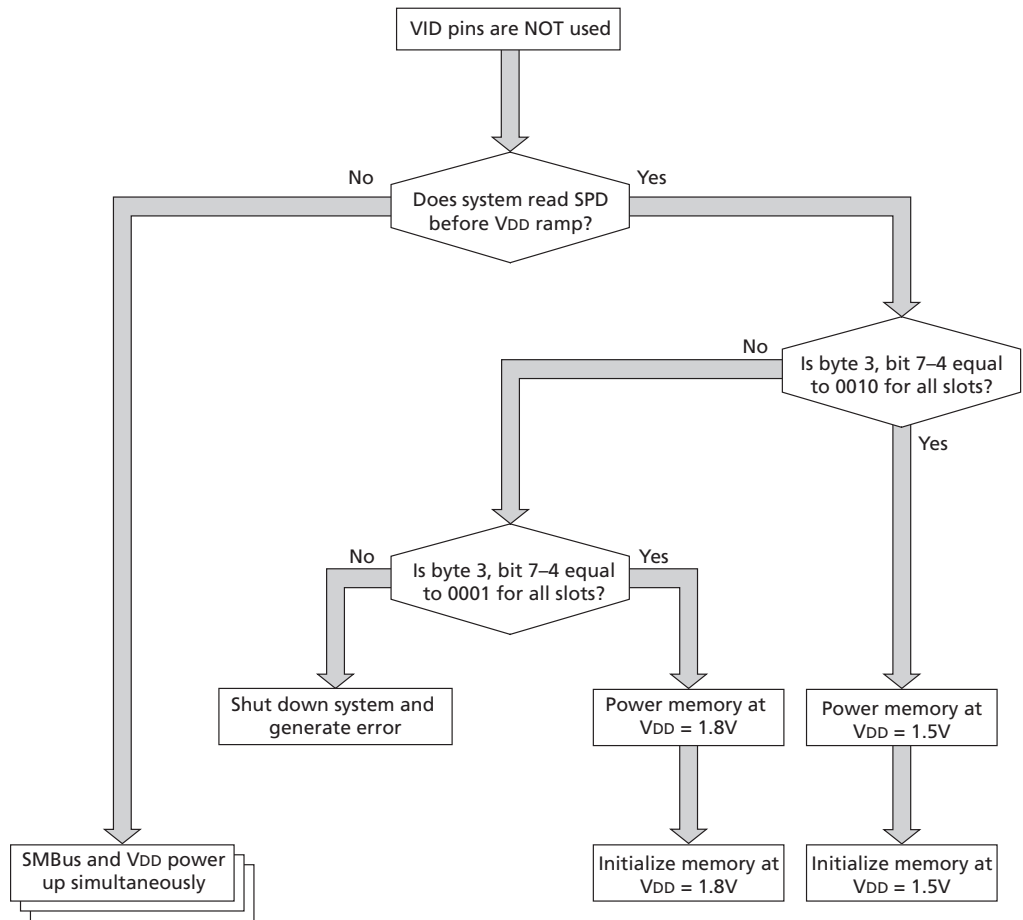
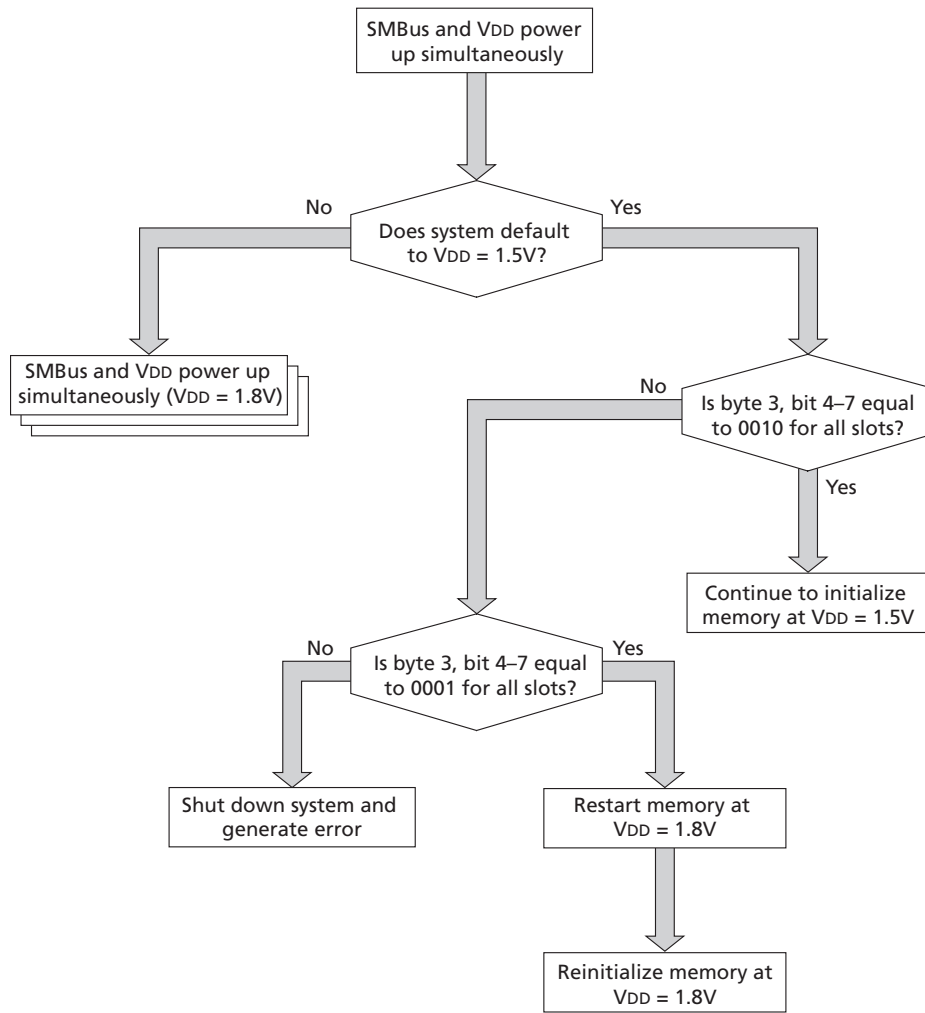
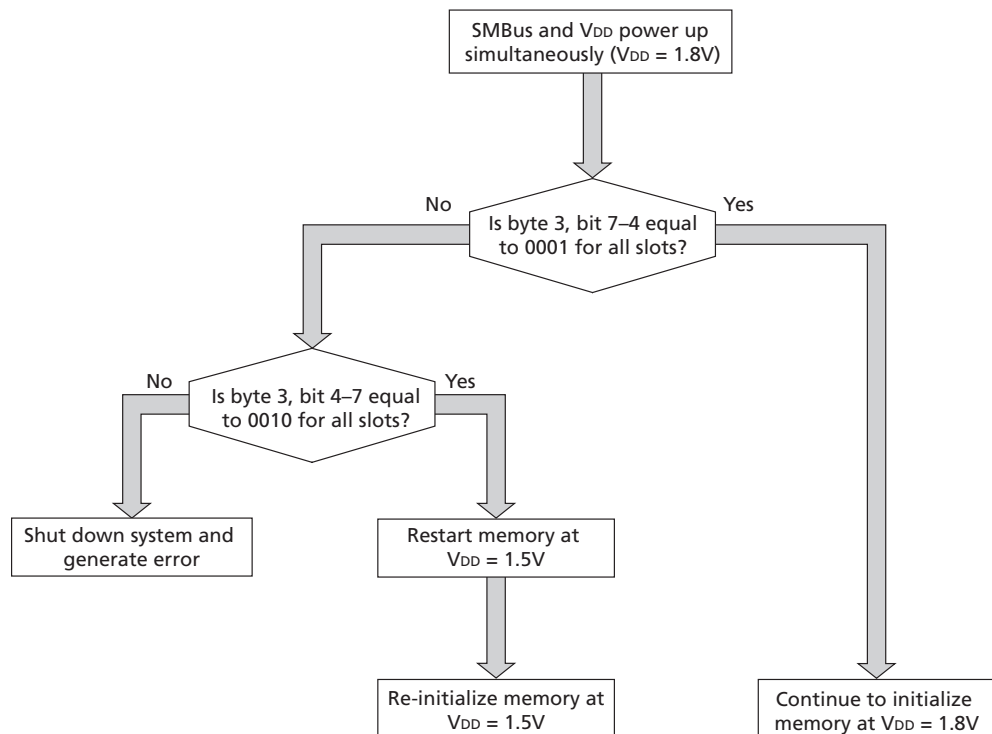


Figure 11: Flowchart Where SMBus and VDD Power Up Simultaneously at 1.5V



**Figure 12: Flowchart Where SMBus and VDD Power Up Simultaneously at 1.8V**


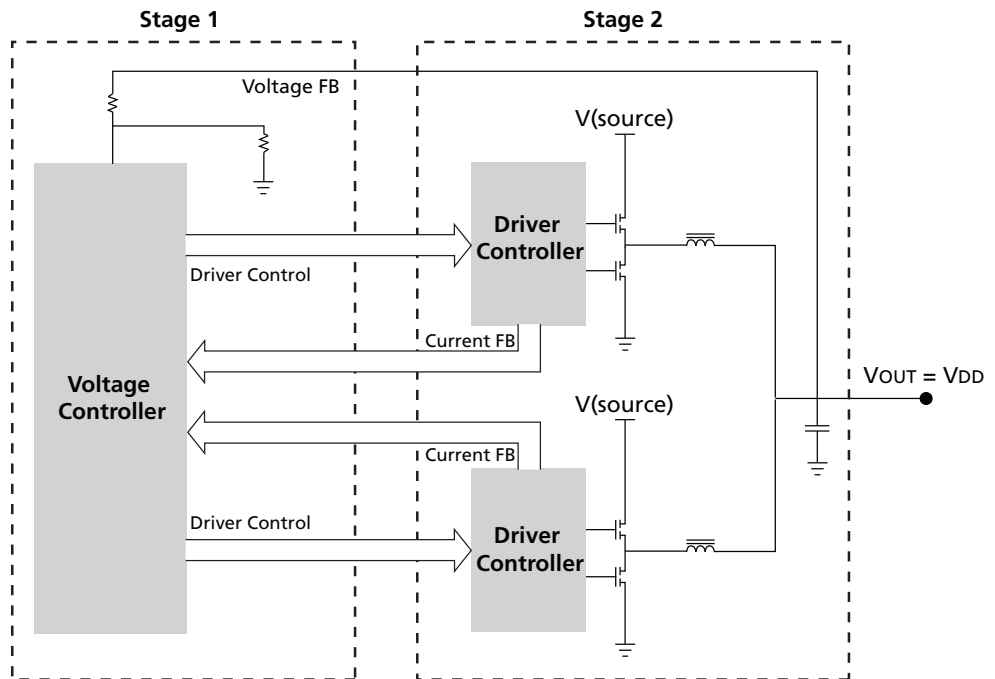
## Hardware Implementation

OUT or VDD) to 1.5V rather than 1.8V. The examples are intended to show the simplicity of the changes and are not meant to be exact guidelines for changing over any platform to support only 1.5V memory.

Typically, memory power is controlled by a high-resolution voltage regulator (first stage) that drives high current output drivers (second stage). Second stage drivers usually include switching type regulators that ensure an even distribution of power through multiple sources. The second stage remains about the same in terms of circuit design, regardless of memory voltage, but varies somewhat by manufacturer or the type of voltage controller used.

Likewise, the primary higher resolution voltage controllers operate about the same between vendors. Each controller has a method for selecting the output voltage level and each has a method for interfacing with the second stage devices. Some first stages will be controlled by an analog circuit that biases the internal circuits for an exact output level. Other first stage controllers will be digitally controlled by logic levels present on input VID pins. Finally, some controllers may rely on a combination of digital and analog techniques for selecting the output voltage level. Any of these methods provide the user with the ability to adjust the output voltage levels.

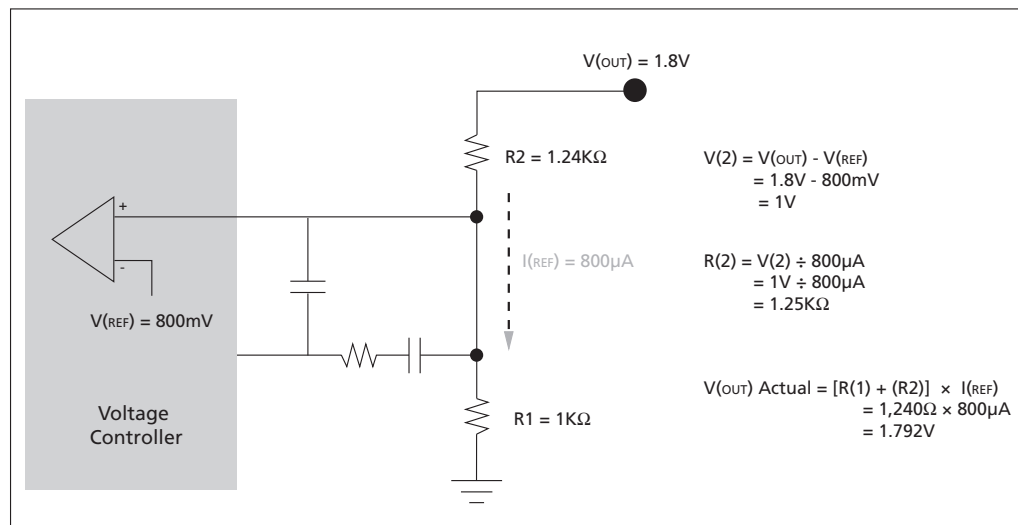
Figure 13: Simplified Block Diagram of the Memory Voltage Controller



## Understanding Analog-Type Voltage Regulators

$800\mu\text{A}$  through it. On the reference side of the  $1.24\text{K}\Omega$  resistor, the voltage level is  $800\text{mV}$ , so with  $800\mu\text{A}$  through the  $1.24\text{K}\Omega$  resistor, the  $V_{\text{OUT}}$  level is  $\sim 1.8\text{V}$  [ $800\text{mV} + (1.24\text{K}\Omega \times 800\mu\text{A})$ ].

## Typical 1.8V Bias for Analog-Type of Controller



For analog-type devices, changing the output drive level (memory voltage) from  $1.8\text{V}$  to  $1.5\text{V}$  is just a matter of changing resistor values on the voltage divider network. We can either use the  $1\text{K}\Omega$  resistor on the lower leg of the network for a constant  $800\mu\text{A}$ , or we can change the lower leg resistor to adjust the current value.

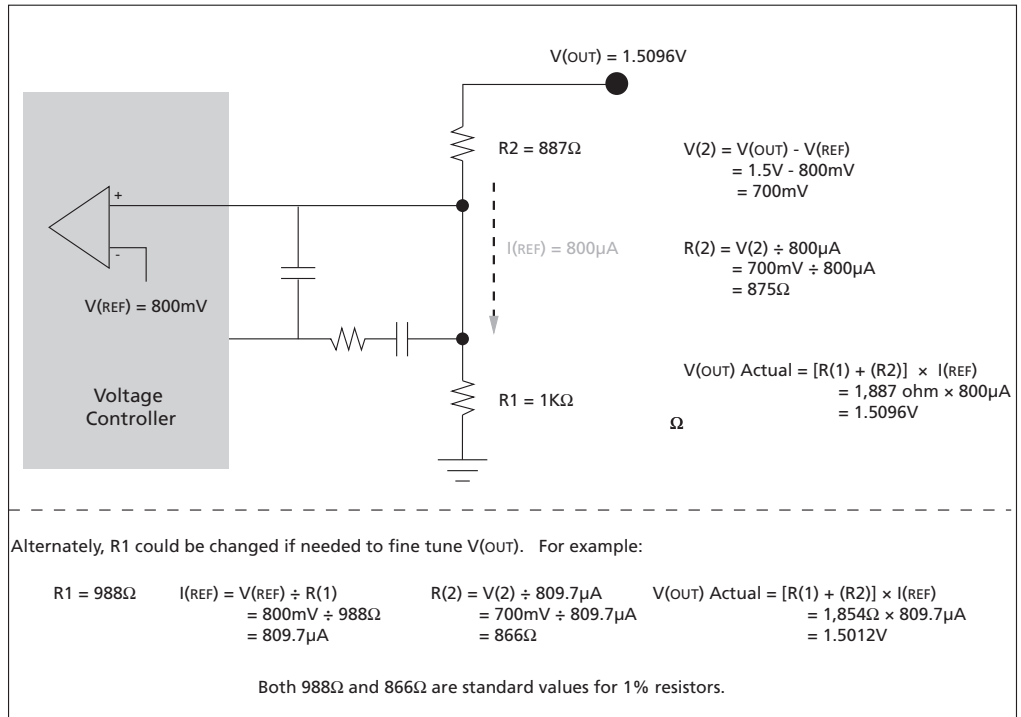
Seeing that a  $1\text{K}\Omega$  resistor is a very common 1% resistor value, for this example, let's assume  $R1$  will continue to be  $1\text{K}\Omega$ . We know the lower leg ( $R1$ ) of the voltage divider will always have  $V1 = 800\text{mV}$ , and if we keep the  $1\text{K}\Omega$  resistor, there will continue to be  $800\mu\text{A}$  of current. We can solve for the value of the top leg ( $R2$ ) of the divider by using Ohm's law:

$$R2 = V2/I2$$

$$\text{where } V2 = 700\text{mV} (1.5\text{V} - 800\text{mV}) \text{ and } I2 = 800\mu\text{A}$$

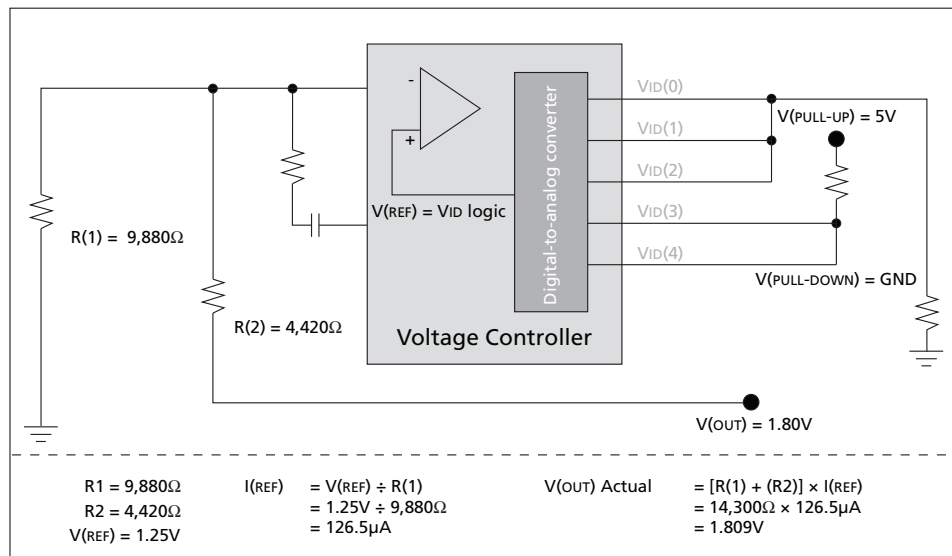
This makes  $R2$  equal to  $875\Omega$ . But  $875\Omega$  is not a standard 1% resistor size (standard sizes include  $866\Omega$  and  $887\Omega$ ).  $V_{(\text{OUT})}$ , using the closest value of  $866\Omega$ , would be  $\sim 1.492\text{V}$ ;  $V_{(\text{OUT})}$ , using  $887\Omega$ , would produce a voltage level of  $\sim 1.5096\text{V}$ . If this value is not precise enough for your design, the value of  $R1$  can be changed as well. Figure 15 illustrates this example of changing an analog-type regulator to provide  $1.5\text{V}$  rather than  $1.8\text{V}$ .

**Figure 15: Example of Changing Analog-Type of Controller to 1.5V**

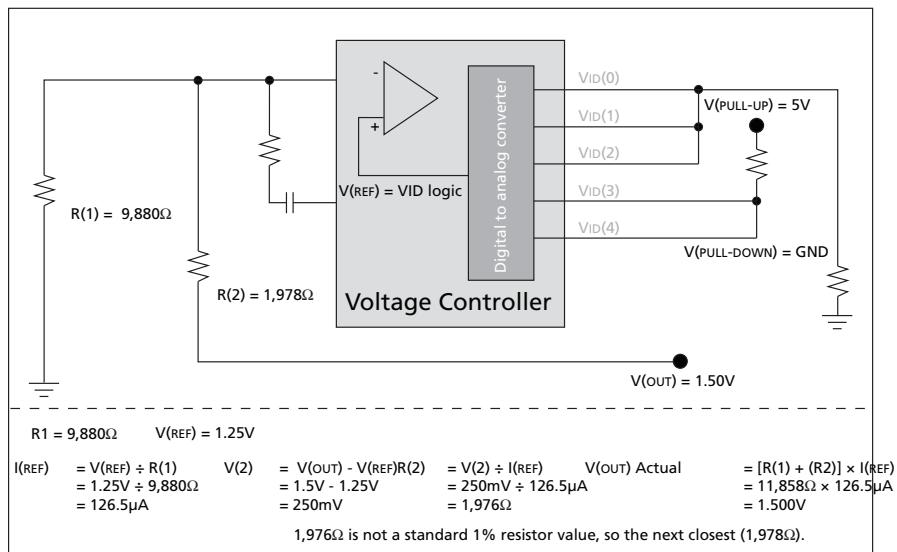


## Changing the Output Voltage on Digital-Type Voltage Regulators

**Figure 16: Example of Digital Controller Set to 1.8V**

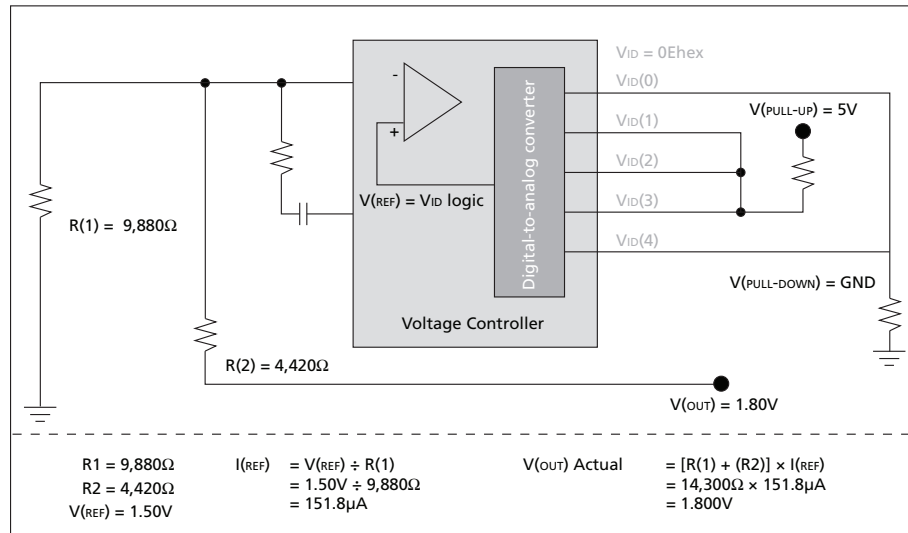


**Figure 17: Example of Changing a Digital Controller to 1.5V Using Different Resistor Values**

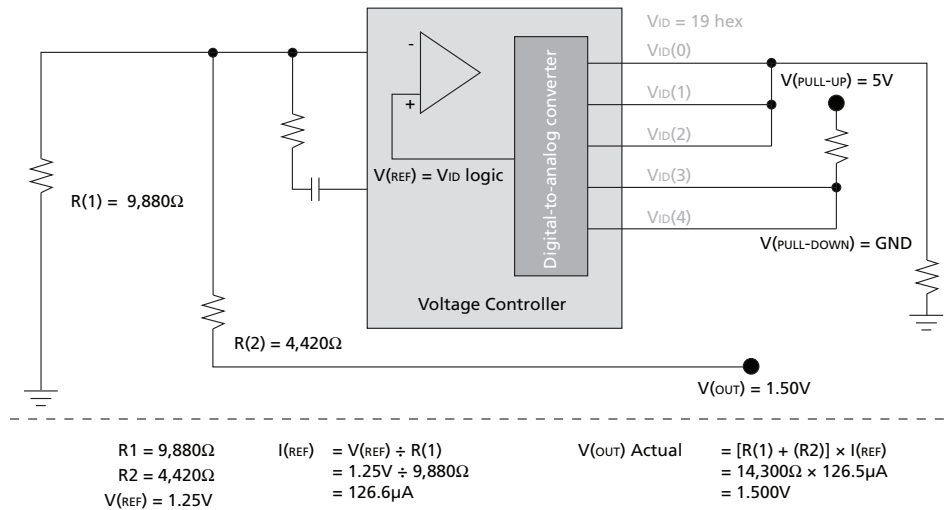


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**Figure 18: Example of Digital Voltage Regulator Set (by VID Pins) to V(out) = 1.8V**



**Figure 19: Example of Setting Memory Voltage (by VID Pins) on a Digital Regulator**





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