



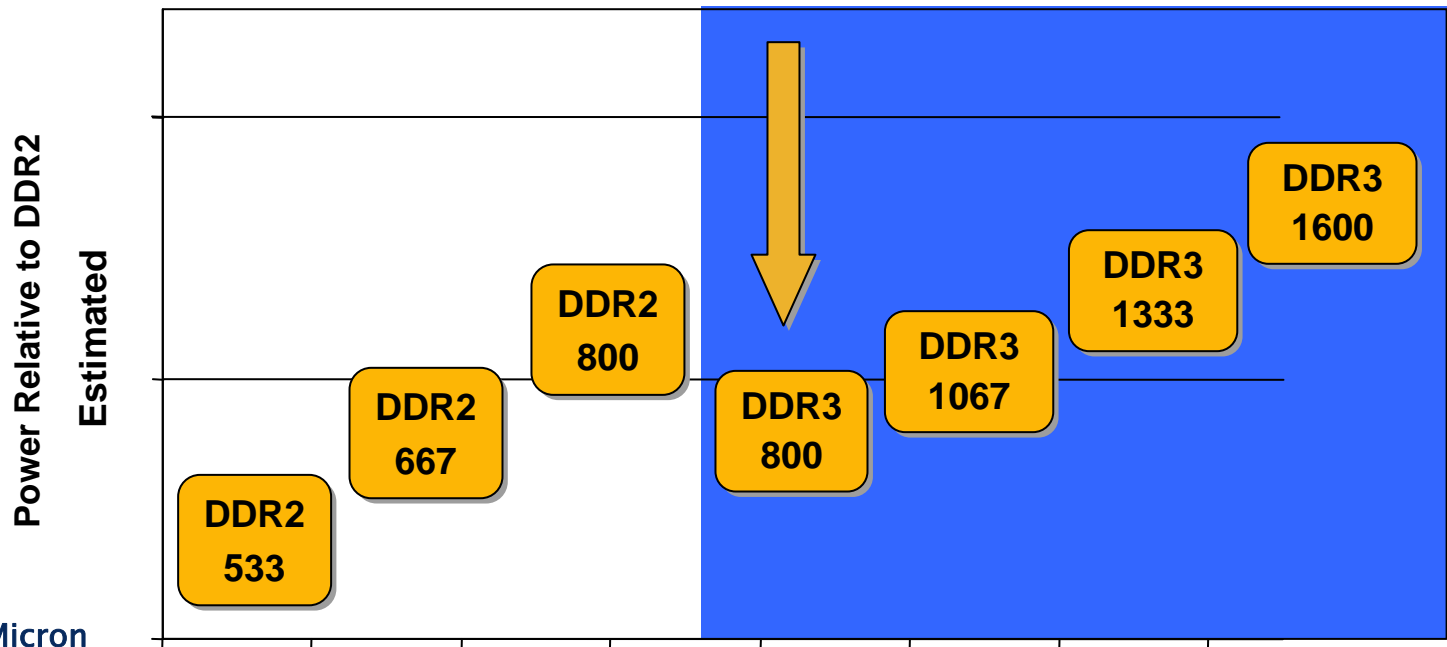
# DDR3 Advantages

# DDR3 Advantages

- Lower power
- Higher speed
- Master reset
- More performance
- Larger densities
- Modules for all applications

# Lower Power

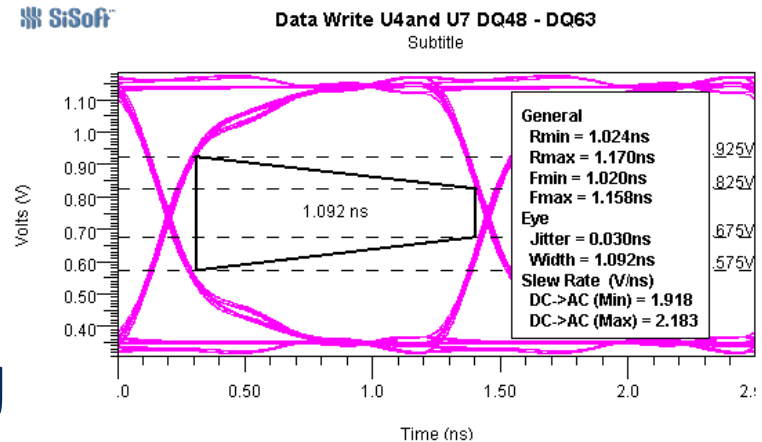
- Supply voltage reduced from 1.8V to 1.5V
  - ~30% reduction in power due to supply voltage alone
- Lower I/O buffer power
  - 34 ohm driver vs. 18 ohm driver



Source: Micron

# Designed for High-Speed Signaling

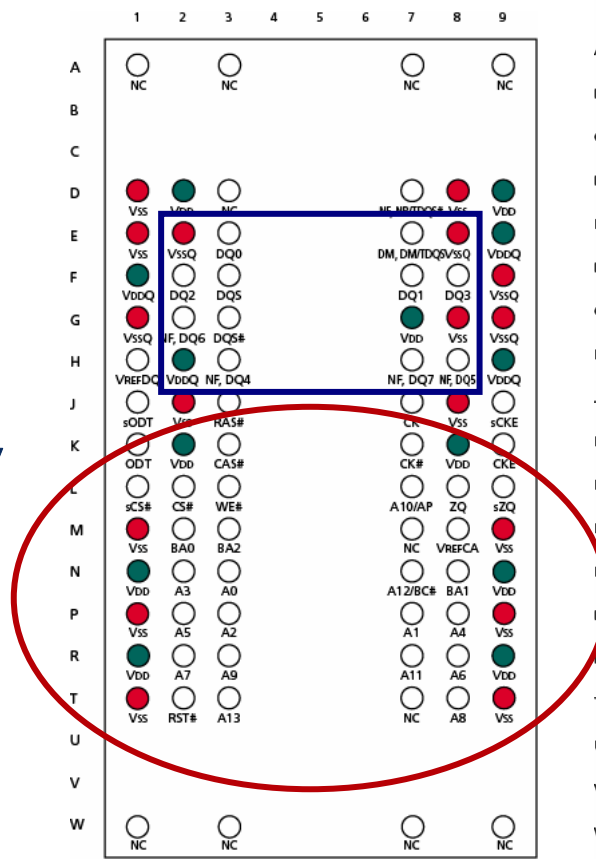
- Improved pinout
- Fly-by architecture
- READ and WRITE leveling
- Data calibration through ZQ resistor
- Dynamic ODT for improved WRITE signaling
- 2 DIMMs/channel at DDR3 frequencies



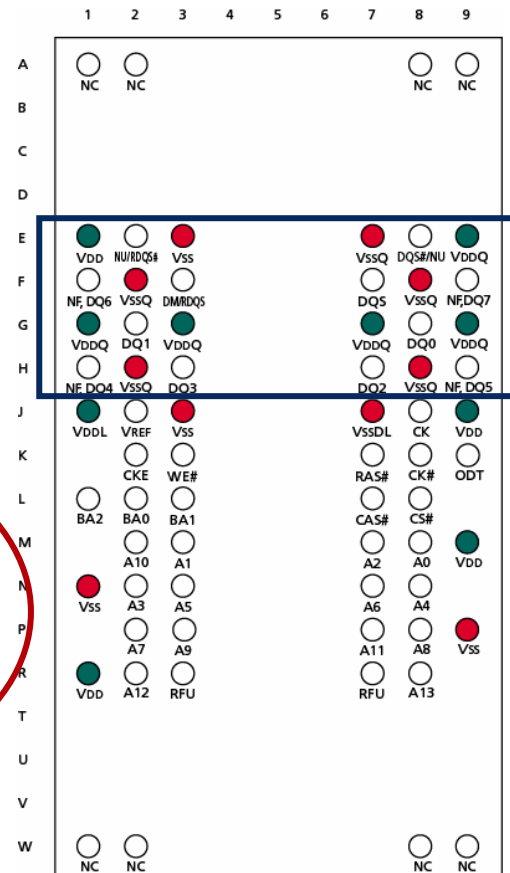
# Improved Pinout

- Improved power delivery
  - ▶ More power and ground balls
- Improved signal quality
  - ▶ Improved signal integrity
  - ▶ Improved power and ground distribution
  - ▶ Improved signal referencing
- Fully populated ball grid
  - ▶ Improved mechanical reliability
- Improved D/Q array
  - ▶ Less D/Q skew
  - ▶ Tighter D/Q timing

## DDR3

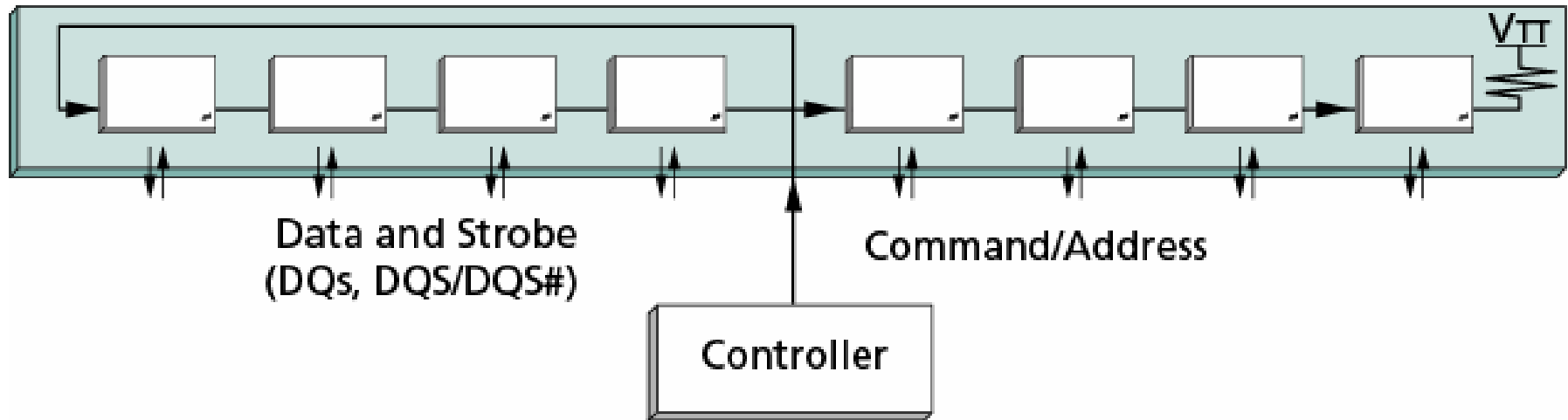


## DDR2



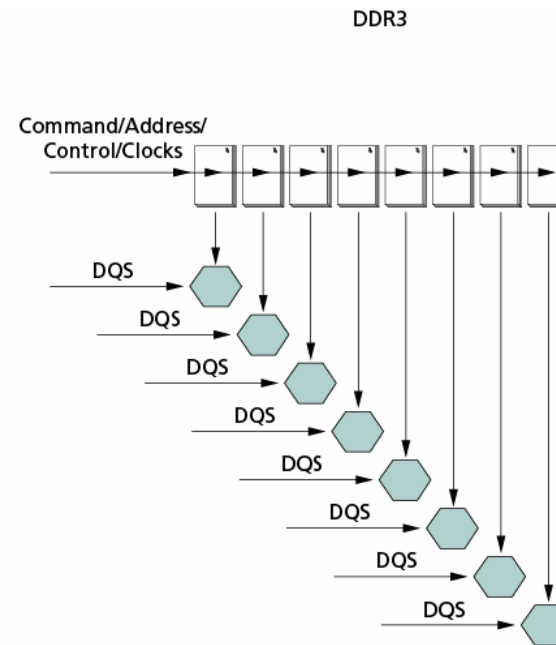
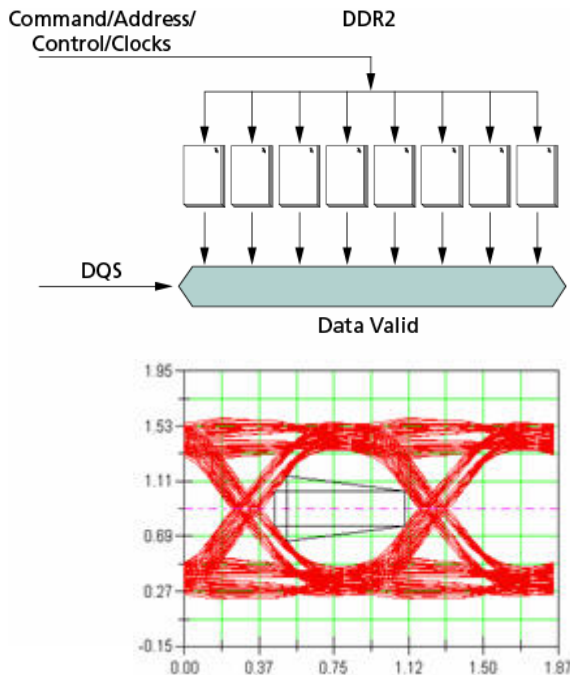
# Improved Module Layout

- Fly-by architecture for C/A, control, clocks
  - Improved signal integrity for high speeds
  - On-module termination
  - Used on UDIMM, SODIMM, RDIMM
- Not used on DDR2 – not needed at lower frequencies



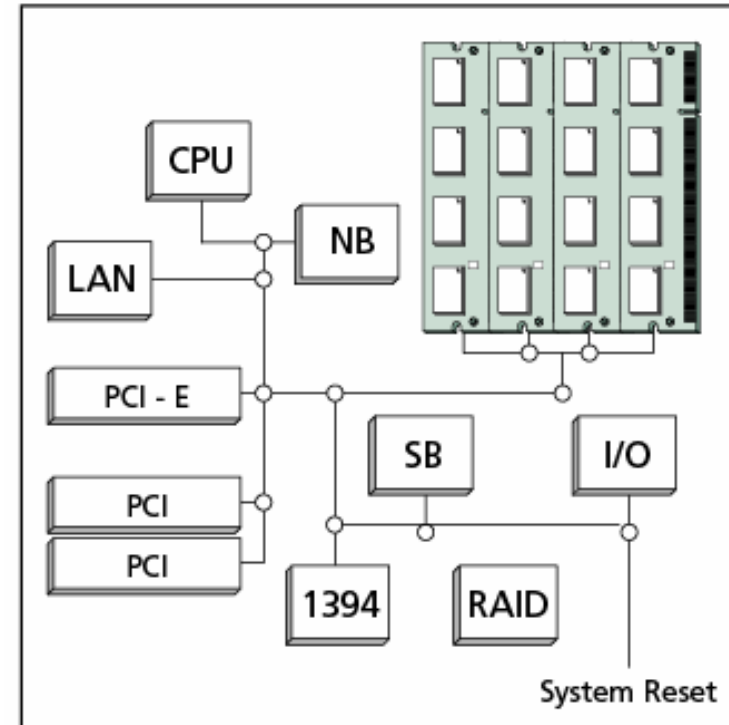
# READ/WRITE Leveling

- Allows for controller to determine the time delta for data command to data output of each DRAM (byte lane)
  - ▶ Enables controller to capture data for each byte lane
  - ▶ Enables controller to adjust receiver timing per byte lane



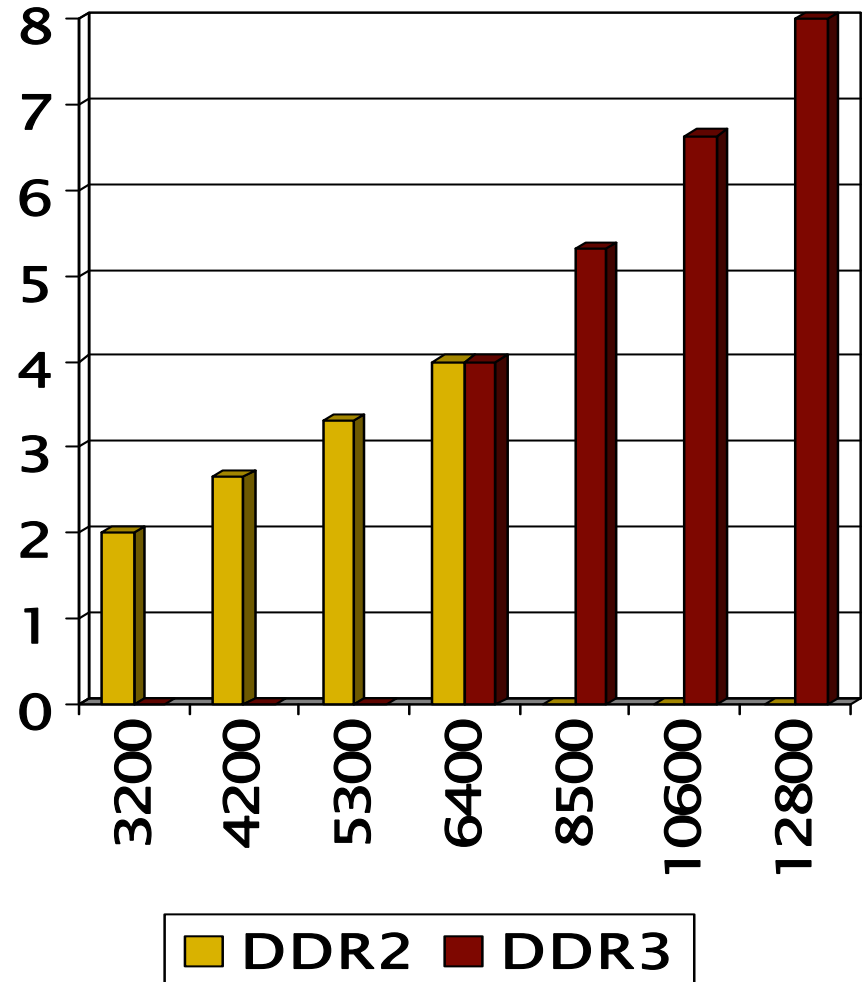
# Master Reset

- Improved system stability
  - ▶ Eliminates unknown start-up states
  - ▶ Known initialization and recovery state
    - Cold boot reset
    - Warm boot reset
    - Removes controller burden to ensure no illegal commands



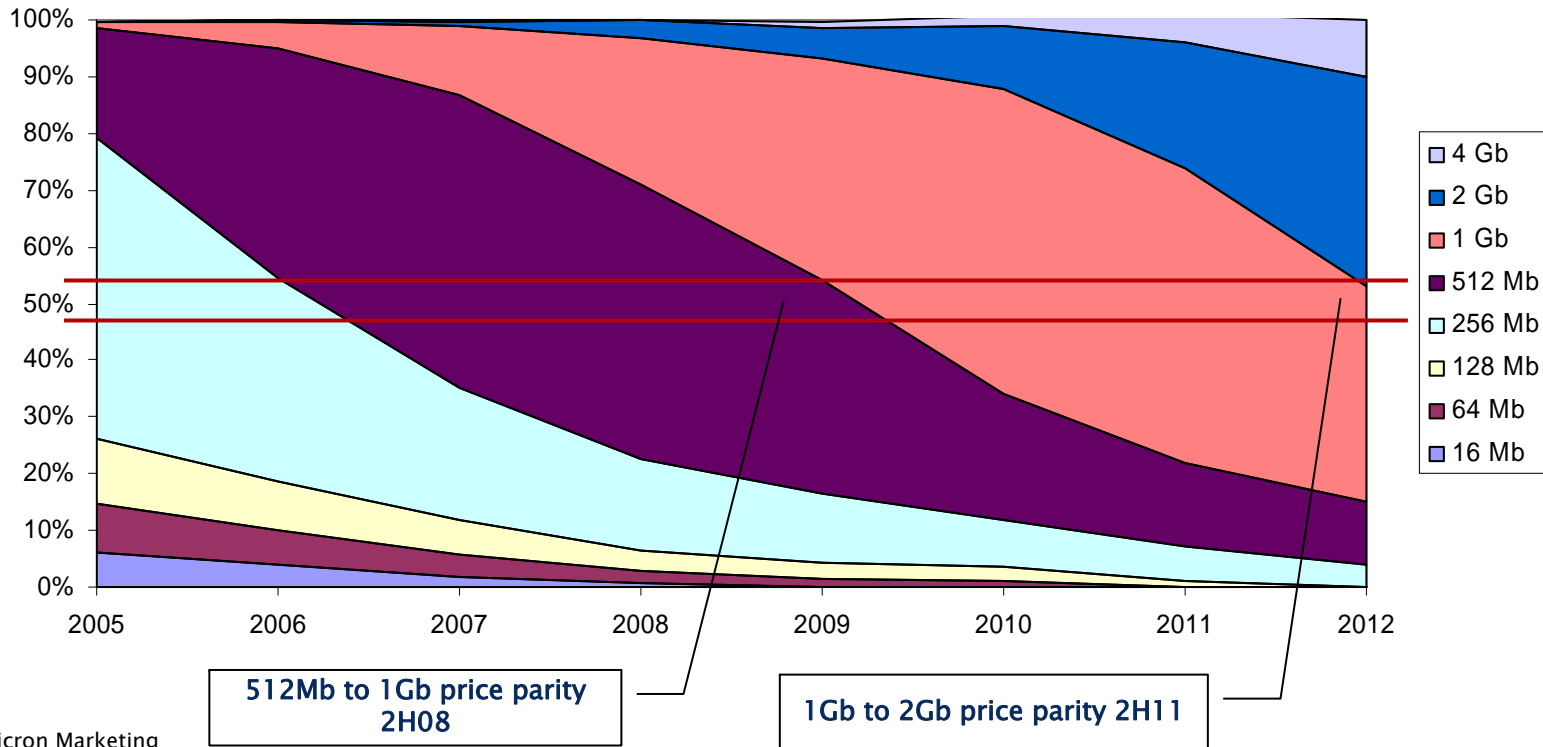
# Increased Peak Performance

- 2X the bandwidth of DDR2
  - ▶ Component per pin
    - 800 MT/s to 1600 MT/s
  - ▶ Bus bandwidth
    - 6400 MT/s to 12,800 MT/s
- 8 banks vs. 4 banks
  - ▶ More open banks for back-to-back access
  - ▶ Hide turnaround time
  - ▶ Hide  $t_{RP}$



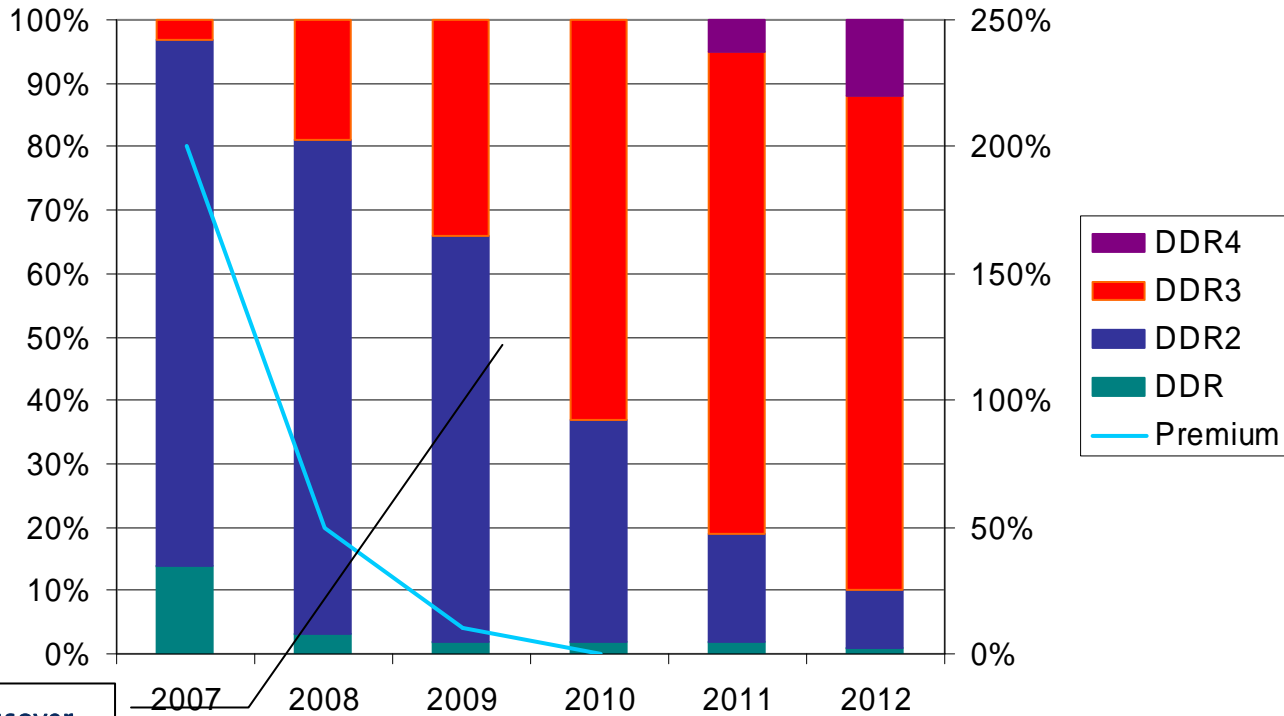
# DDR3 Market

- DDR3 market dynamics
  - ▶ 512Mb/1Gb crossover
  - ▶ 1Gb/2Gb crossover
  - ▶ DDR3 life from 2007 through 2014



Source: Micron Marketing

# DDR3 Ramp



Source: Micron Marketing

DDR2 to DDR3 Crossover

	2007	2008	2009	2010
DDR	14%	3%	2%	1%
DDR2	83%	78%	64%	33%
DDR3	3%	19%	34%	60%

# Maximum\* Module Density

Component Density / Module Density		256Mb	512Mb	1Gb	2Gb	4Gb	8Gb
<b>DDR2</b>	UDIMM (18)	512MB	1GB	2 GB	4 GB	n/a**	n/a
	SODIMM(16)	512MB	1GB	2 GB	4 GB		
	RDIMM(36)	1GB	2 GB	4GB	8 GB		
	FBDIMM(36)	1 GB	2GB	4 GB	8GB		
<b>DDR3</b>	UDIMM (18)	n/a	1GB	2 GB	4 GB	8 GB	16 GB
	SODIMM(16)		1GB	2 GB	4 GB	8 GB	16 GB
	RDIMM(36)		2 GB	4 GB	8 GB	16GB	32GB
	FBDIMM(36)		2 GB	4 GB	8GB	16GB	32GB

\*Maximum density requires stacked and/or high component count planar versions of modules

\*\* 4Gb is a JEDEC standard; Micron has no plans to support it

# DDR3 Modules for All Applications

Unbuffered DIMM

	1H07	2H07	1H08	2H08	1H09	2H09
Desktop	Unbuffered DIMM					
Notebook			Small Outline DIMM			
Server				Registered DIMM		
				Fully Buffered DIMM		
Networking					Very Low Profile DIMM	

# Summary

- **DDR3 provides more bandwidth at lower power**
- **Package, pinout, and signaling improvements for higher-speed operation**
- **Master reset for improved system stability**
- **Larger densities**
- **Modules for all applications**

The logo features a stylized white 'M' with a white orbital ring around it, followed by the word 'micron' in a lowercase, bold, sans-serif font. A registered trademark symbol (®) is located at the top right of the word.

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