



Improving Enterprise System Performance With a New Breed of NAND Flash

[Jim Cooke](#)

[Senior Technical Marketing Manager](#)

[Micron Technology](#)

STORAGE VISIONS® 2011
AN ENTERTAINMENT STORAGE ALLIANCE™ EVENT



Agenda

- Abstract
- The Need for ClearNAND™ Flash
- Enhanced ClearNAND Flash Features and Benefits
 - Volume-Addressing Feature
 - Electronic DQ Mirroring
 - Interrupt Function
 - Internal Copyback
- Summary

Abstract

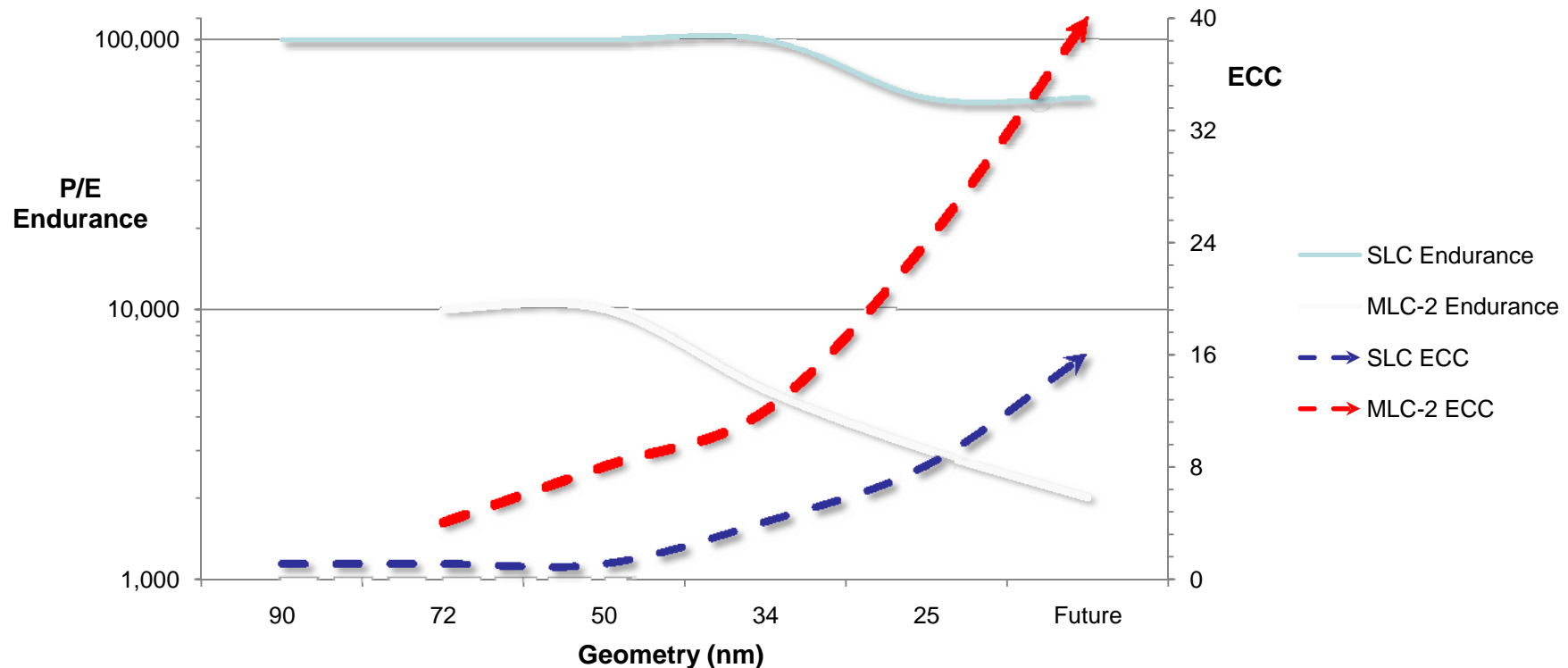
While NAND Flash memory is not new to the enterprise storage market, traditional NAND can present design and performance challenges. While enterprise systems can address these challenges, solutions come at a price—longer design times and larger gate counts due to the increased complexity of the system. In addition, a typical enterprise controller can waste hundreds of signals in controlling an array of traditional NAND devices.

Micron is changing the game with the development of a new class of NAND Flash devices designed specifically for enterprise markets. These new ClearNAND Flash devices allow for more cost-effective and higher-performance controllers by saving hundreds of signals and potentially millions of logic gates.

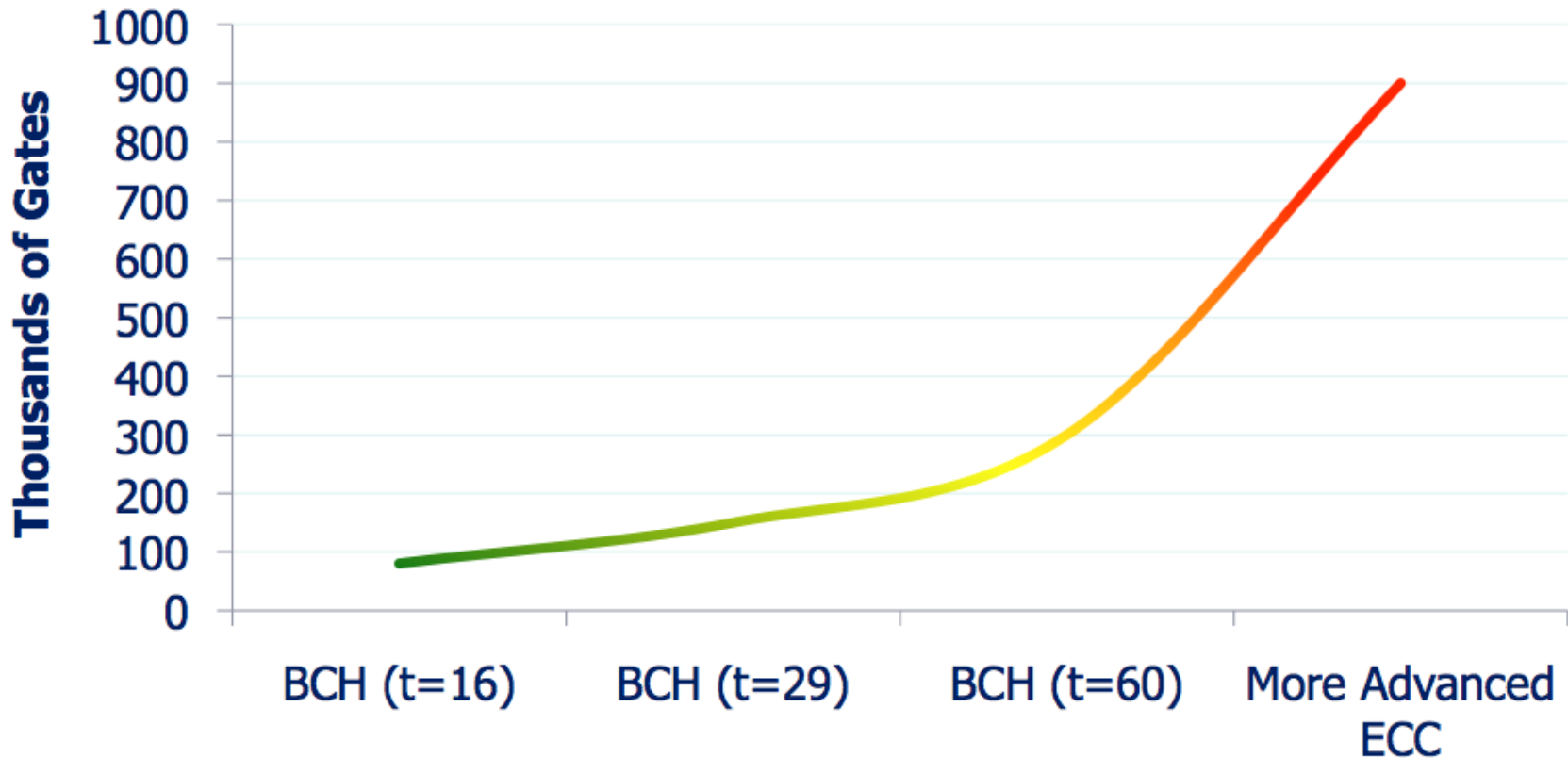
The Need for ClearNAND™ Flash Technology

Endurance and ECC Trends

- Process shrinks lead to fewer electrons per floating gate
- ECC is used to improve data retention and endurance
- To adjust for increasing RBERs, ECC is increasing exponentially to achieve equivalent UBERs

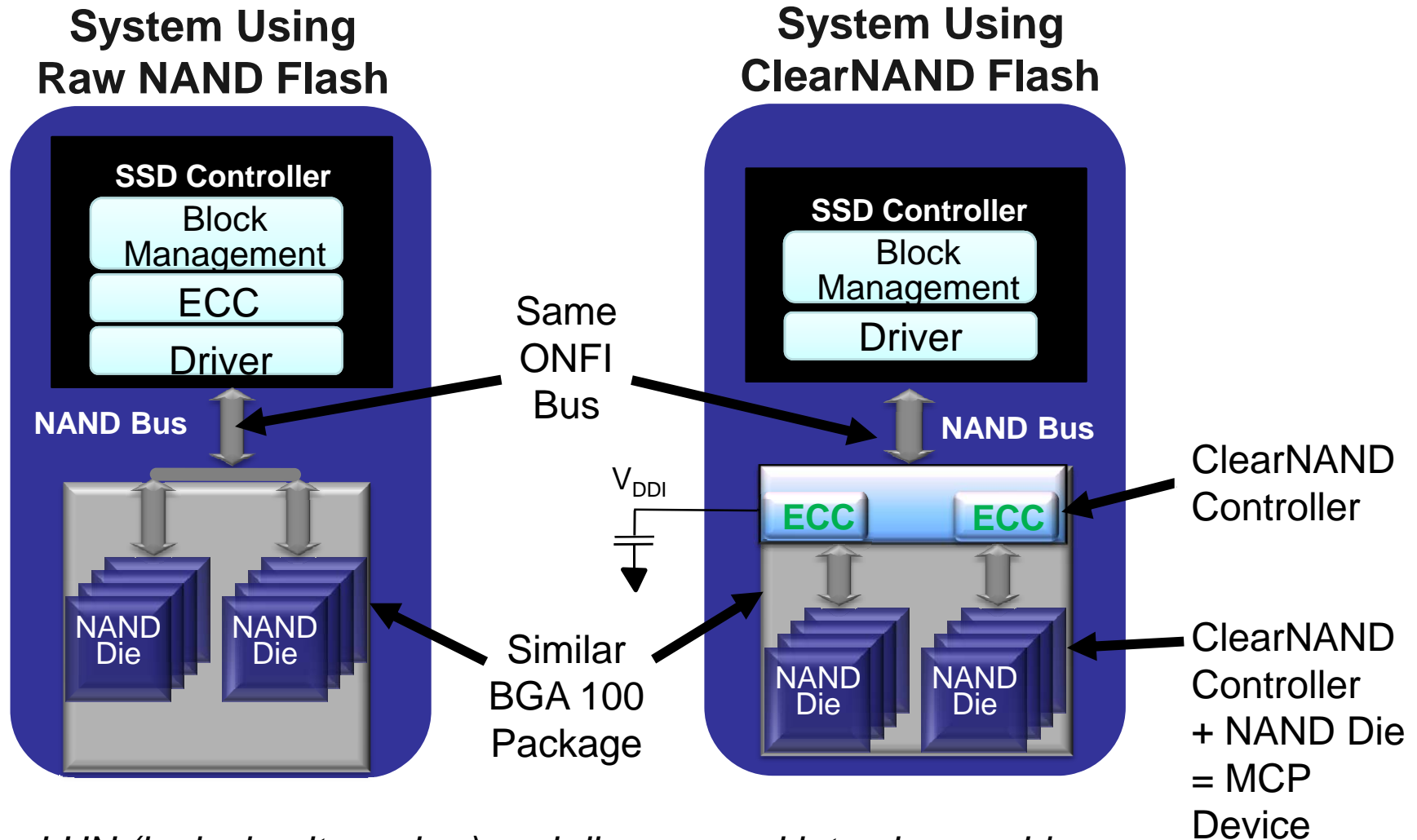


ECC Complexity vs. Logic



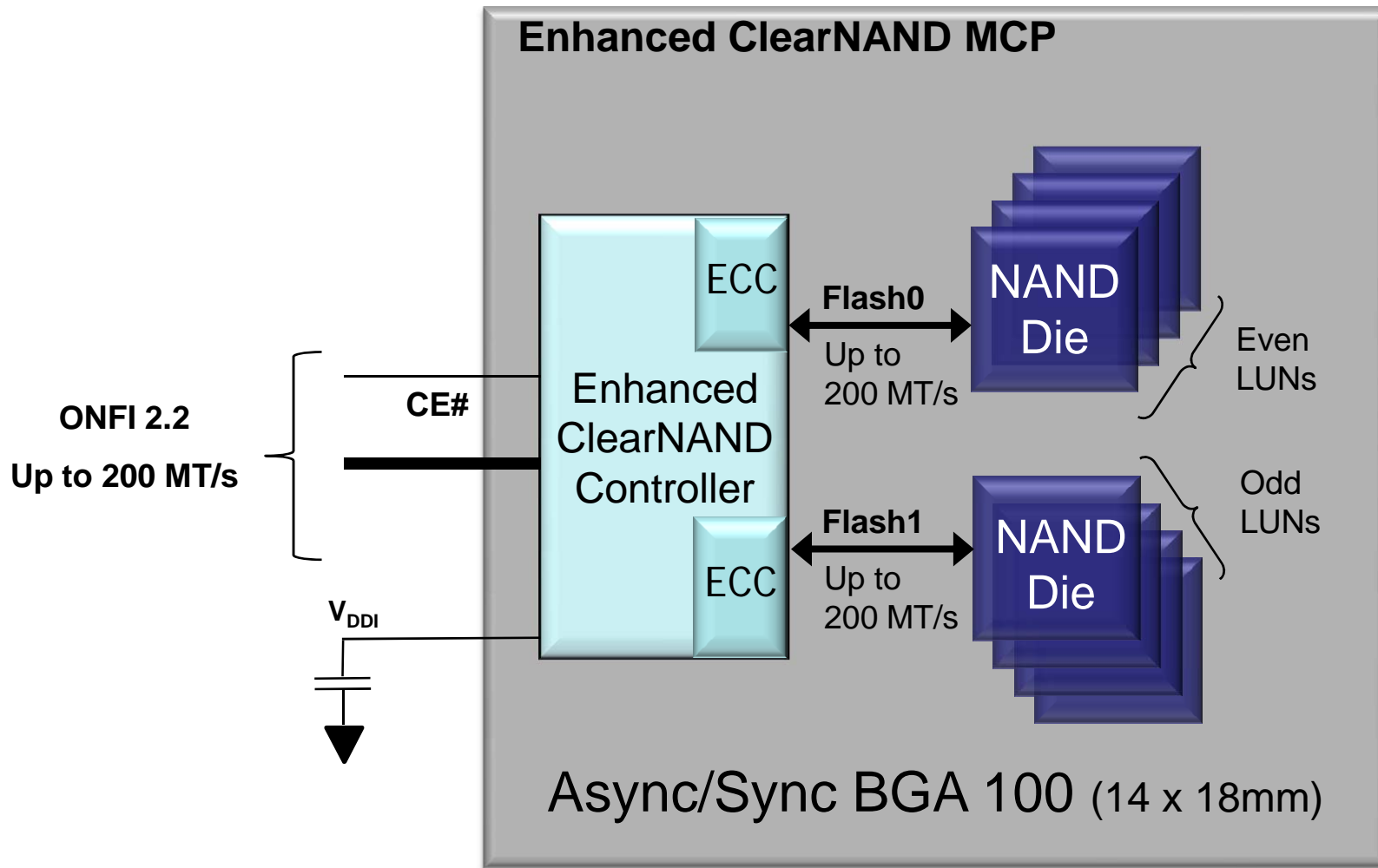
- As ECC increases, the number of logic gates required to implement it also increases
- For high-performance systems, most implementations will use one ECC engine per channel
- For FPGA implementations, these gates are expensive

Raw NAND vs. ClearNAND Flash



Note: LUN (logical unit number) and die are used interchangeably.

Enhanced ClearNAND Flash Architecture

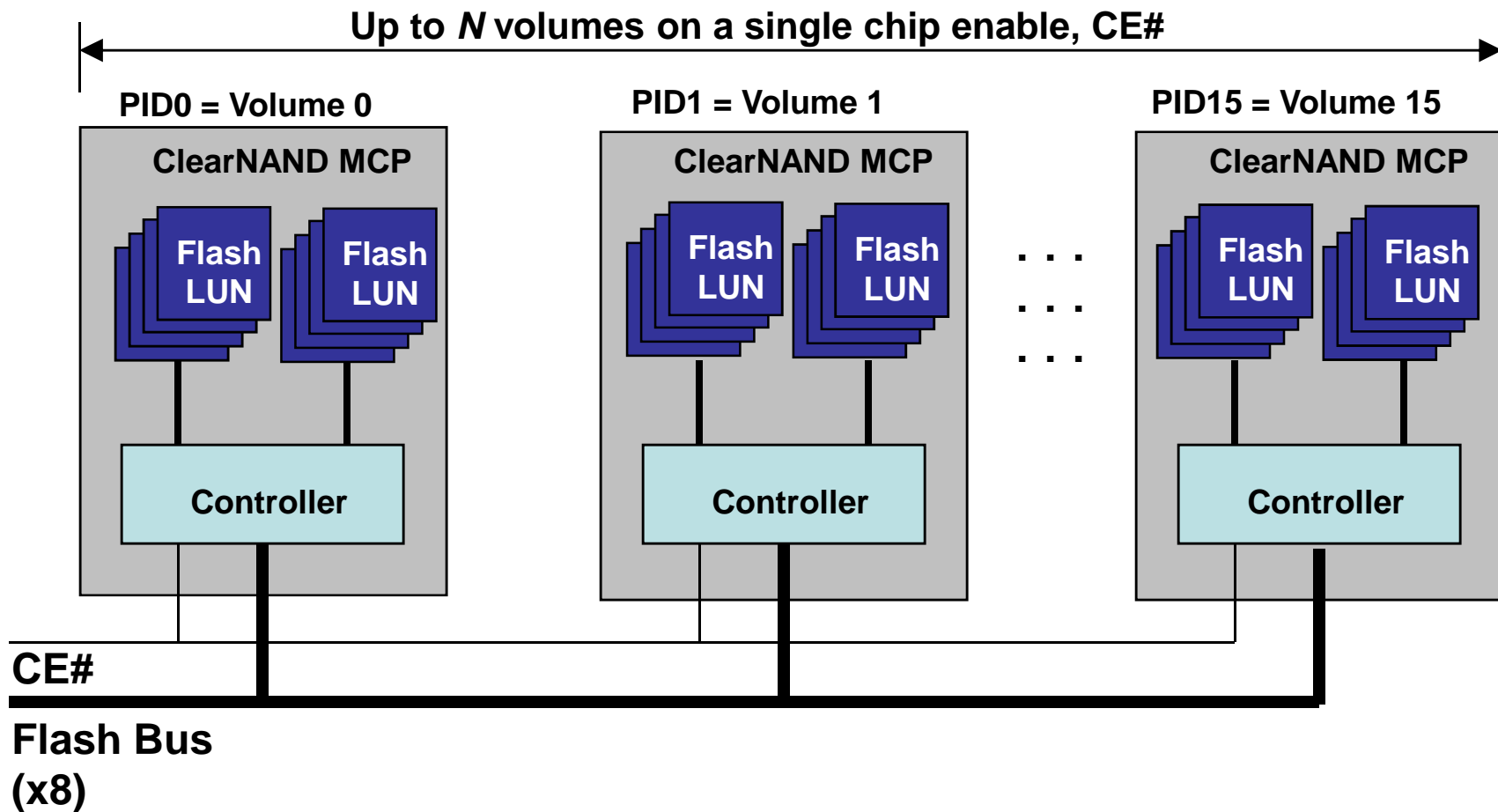


Enhanced ClearNAND Flash Features

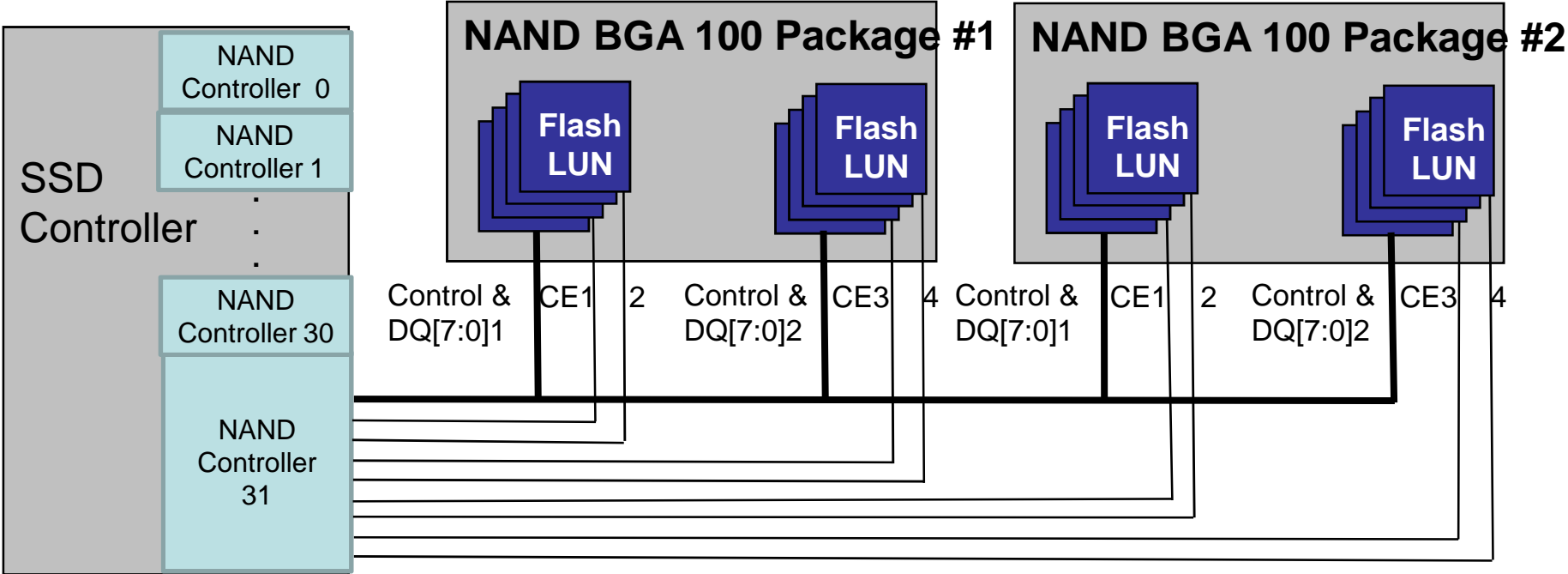
Feature	Benefit
Controller manages ECC and buffers NAND	Allows 128 die per channel— 8x density improvement
ONFI synch interface	High-speed performance; future-proof with ONFI 3 development (400 MT/s)
Volume addressing	Saves hundreds of pins (allows 128 die per channel on a single CE)
Electronic DQ mirroring	Simplified PCB routing and inventory
Interrupt signal	Real-time status updates; more efficient power use
Improved copyback	Achieve better performance by offloading some wear-leveling operations

Volume-Addressing Feature

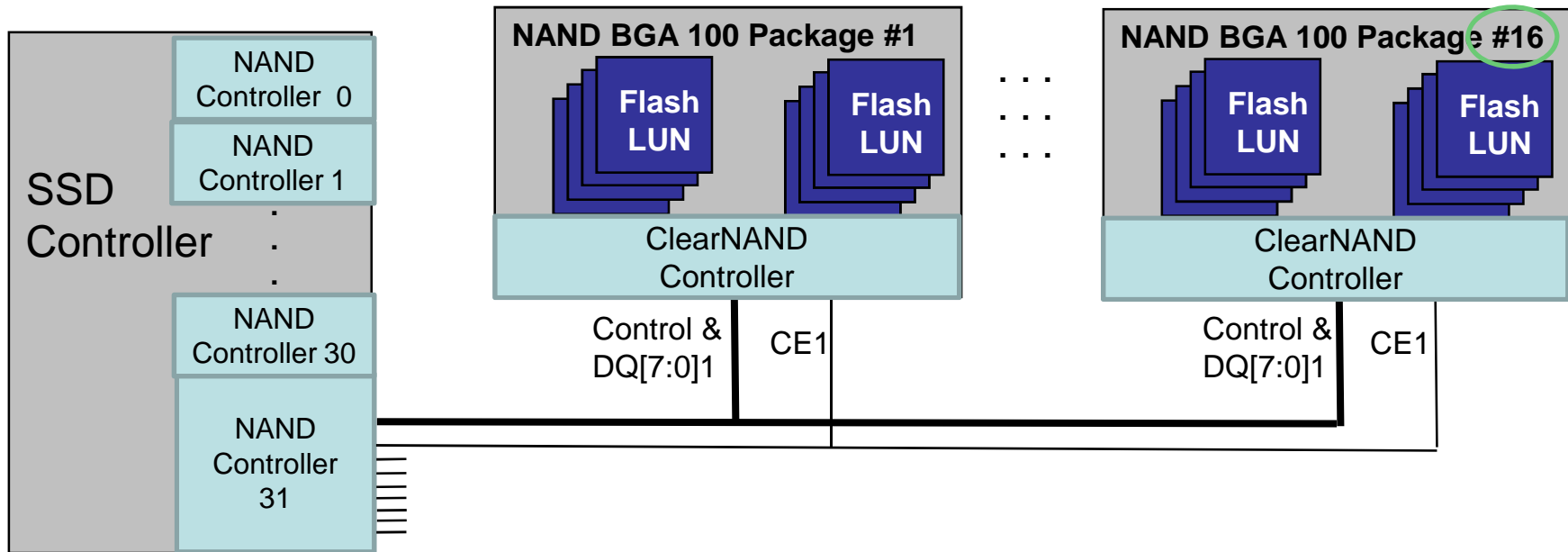
Volume-Addressing Concept



Comparison Using Standard NAND CEs

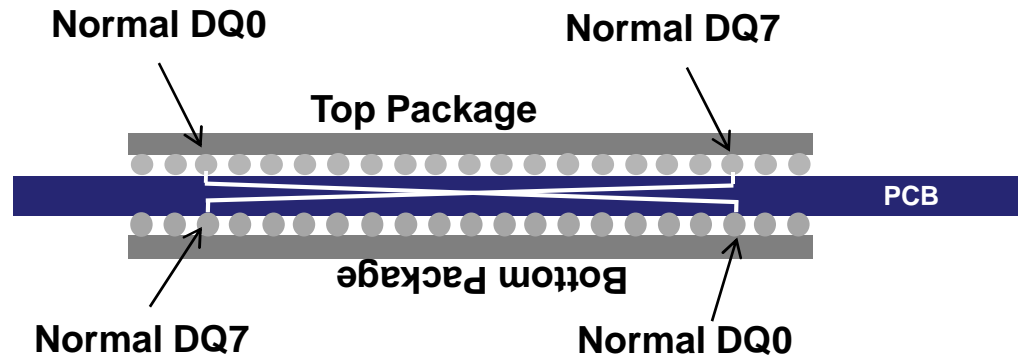
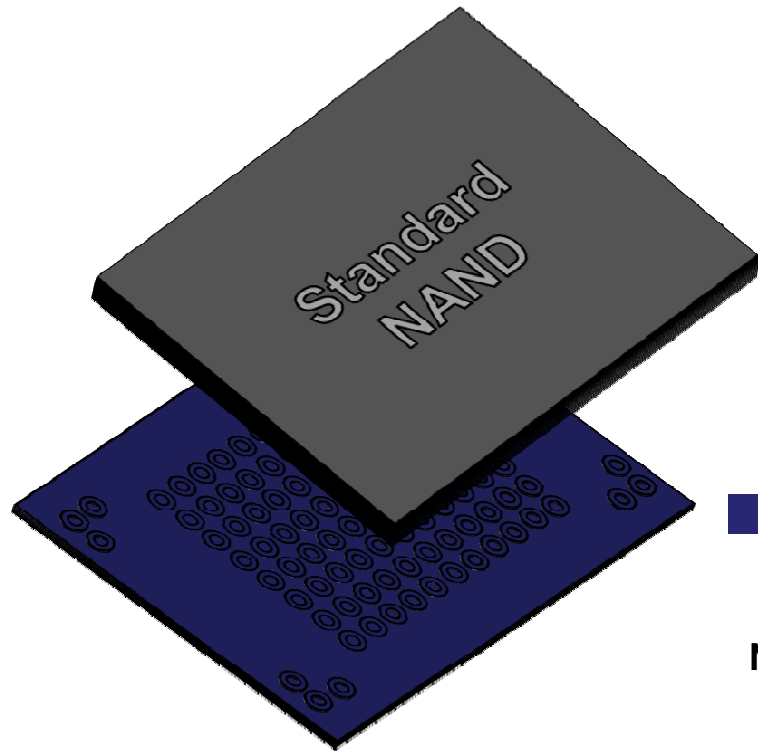


Comparison Using Volume Addressing



Electronic DQ Mirroring

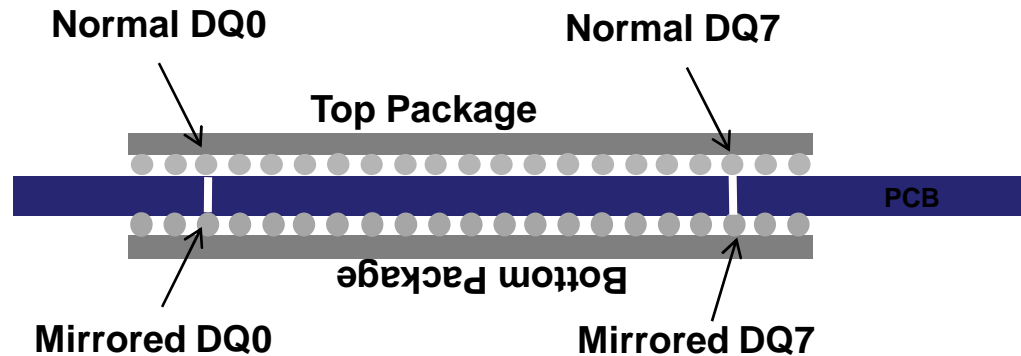
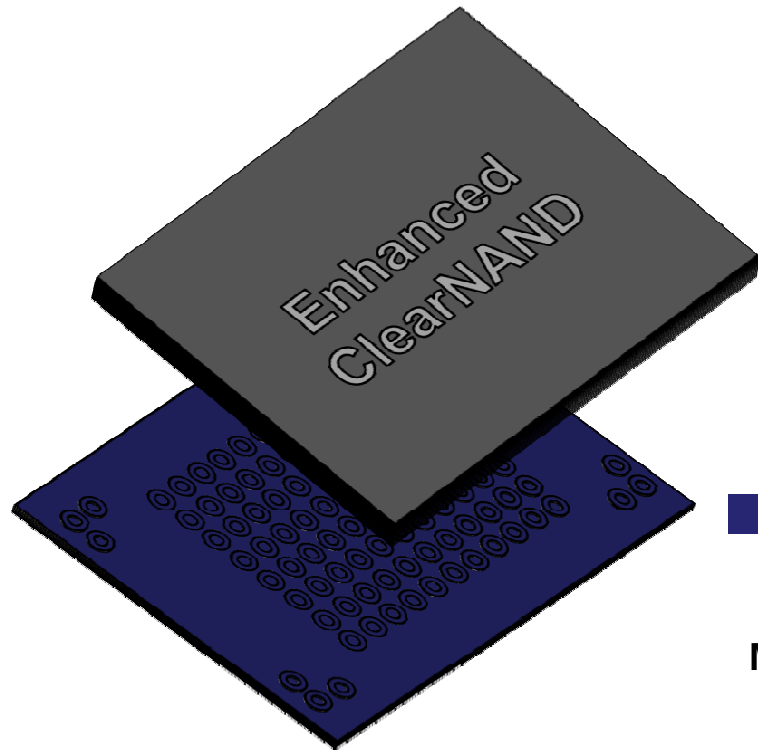
Double-Sided Boards *Without* Electronic Data Mirroring



Problems:

- Non-optimized PCB routing
- Compromised signal integrity

Double-Sided Boards *With* Electronic Data Mirroring

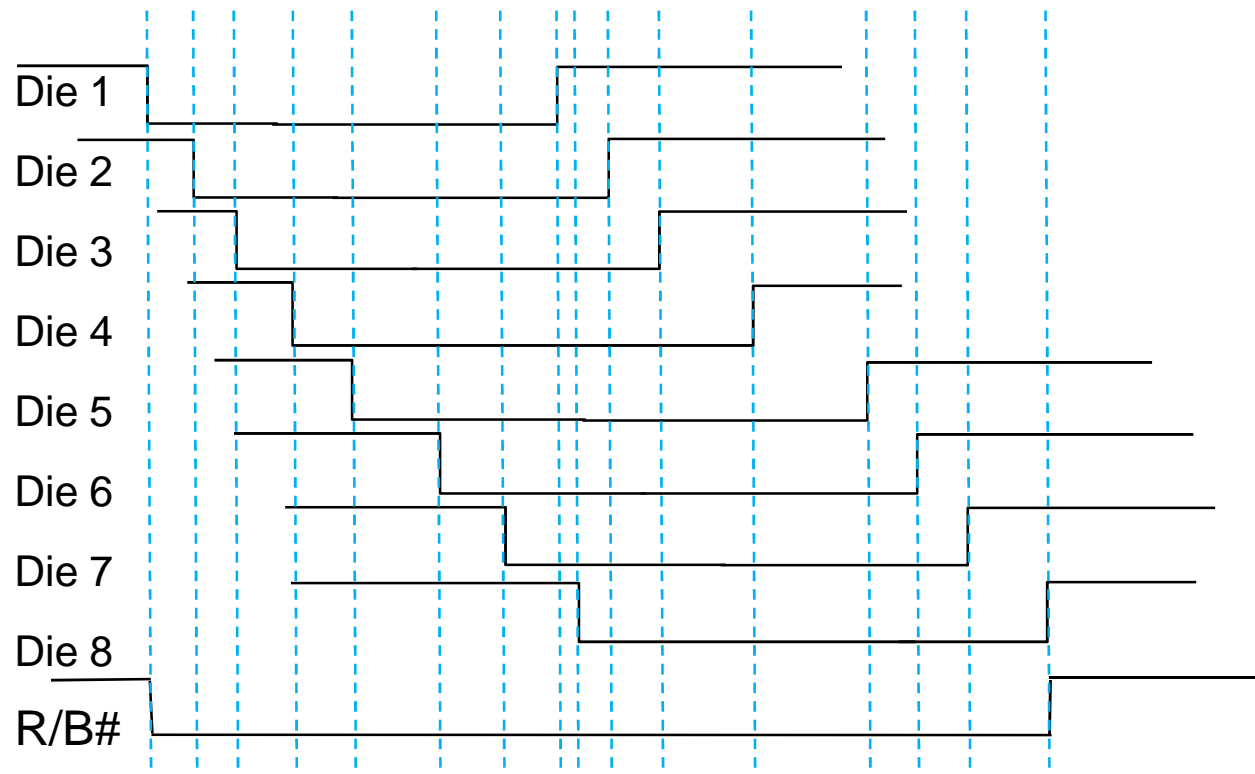


Benefits:

- Simplified PCB routing
- Improved signal integrity

Interrupt Function

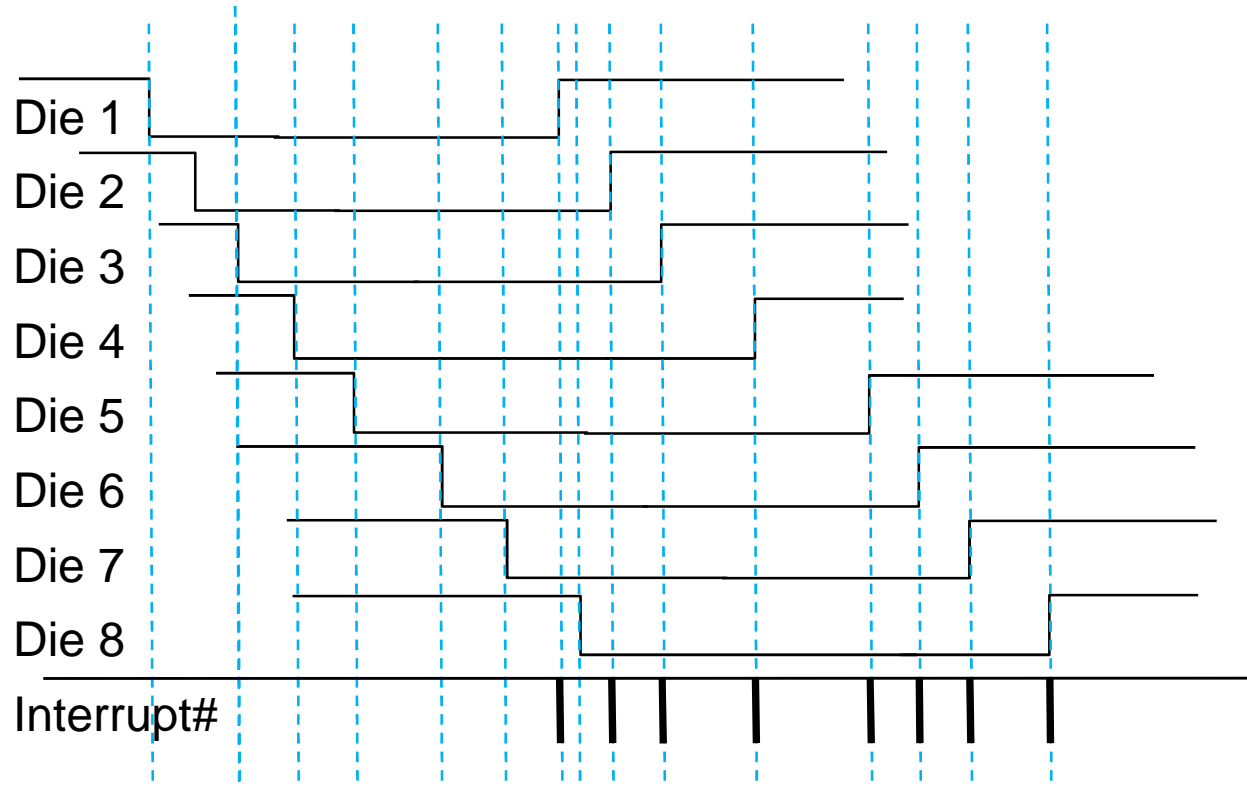
NAND Ready/Busy# (when tied together)



Problems:

- R/B# pin is unmanageable for large systems
- Firmware polls the die for competition status
- Polling wastes power and affects performance

ClearNAND Interrupt Function

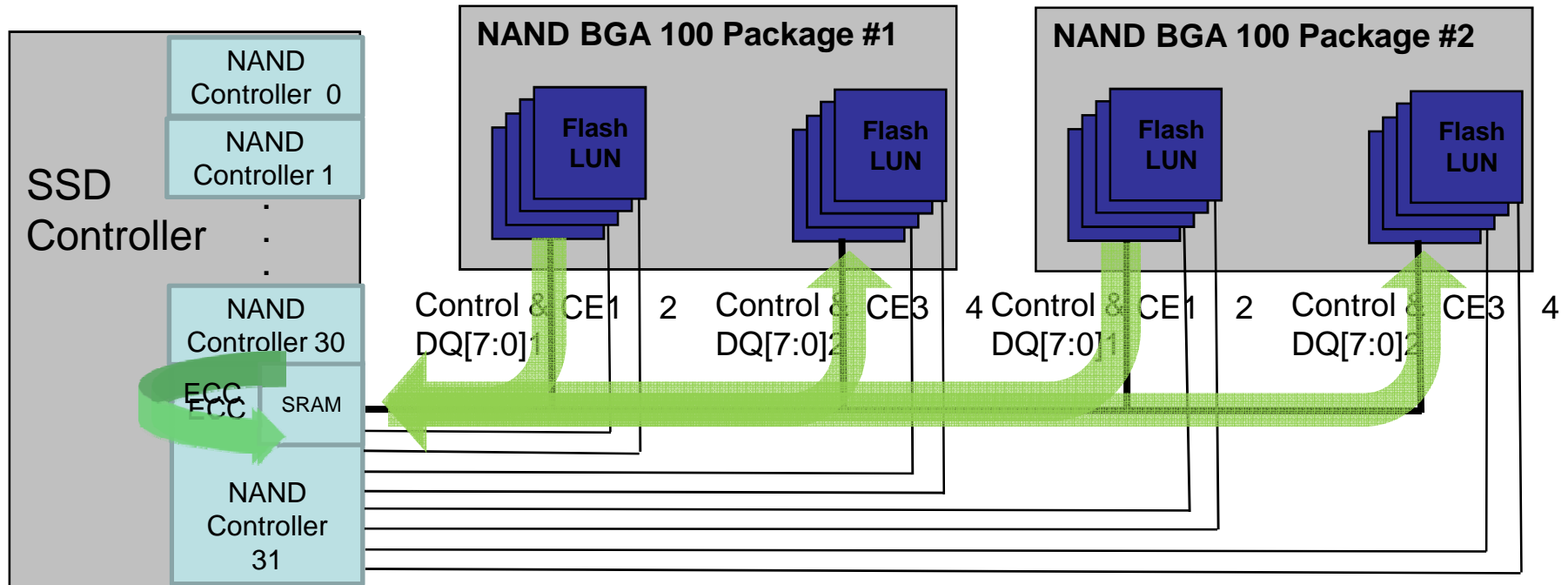


Benefits:

- R/B# pin is redefined to be an interrupt (still open-drain)
- Interrupt pin provides a real-time status when die or volumes become available

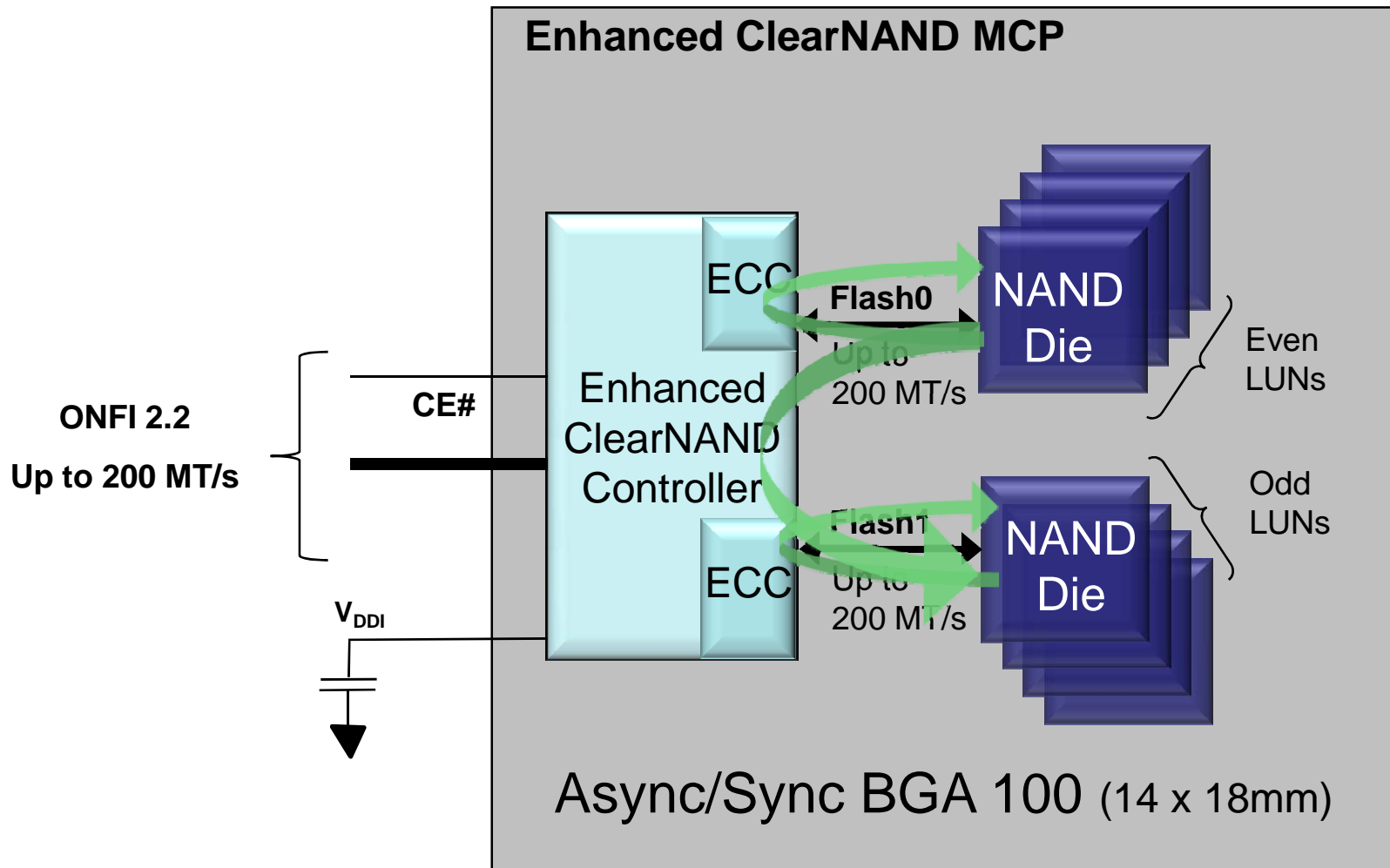
Internal Copyback

Copyback Using Raw NAND



- The following operations are sequential; each must be managed by the SSD controller:
 1. The SSD controller must issue a READ to a single die
 2. The SSD controller completes the ECC correction
 3. The SSD controller PROGRAMS the data back
- The ONFI channel is tied up for this operation

Copyback Using Enhanced ClearNAND



Copyback Among 16 Packages



- Enhanced ClearNAND Flash potentially allows simultaneous operations within each package
- Some percentage of operations may need to go between packages
- Some percentage of operations may need to go between channels
- Copyback efficiency can provide a big benefit for wear-leveling performance

Enhanced ClearNAND Benefits Summary

Feature	Benefit
Controller manages ECC and buffers NAND	Allows 128 die per channel— 8x density improvement
ONFI synch interface	High-speed performance; future-proof with ONFI 3 development (400 MT/s)
Volume addressing	Saves hundreds of pins (allows 128 die per channel on a single CE)
Electronic DQ mirroring	Simplified PCB routing and inventory
Interrupt signal	Real-time status updates; more efficient power use
Improved copyback	Achieve better performance by offloading some wear-leveling operations



Standardization Efforts

- ONFI 3.0 doubles bus speed to 400 MT/s
- Working with ONFI to include these enhanced features as part of an upcoming ONFI specification
- ONFI is also working with JEDEC to include ONFI specifications into the JEDEC organization
- Visit ONFI.ORG for the latest details

For more information, please visit:

www.micron.com/ClearNAND

www.ONFI.ORG

©2010 Micron Technology, Inc. All rights reserved. Products are warranted only to meet Micron's production data sheet specifications. Information, products, and/or specifications are subject to change without notice. All information is provided on an "AS IS" basis without warranties of any kind. Dates are estimates only. Drawings are not to scale. Micron, ClearNAND, and the Micron logo are trademarks of Micron Technology, Inc. All other trademarks are the property of their respective owners.

