



Customer Service Note

BGA Manufacturer's User Guide for Micron BGA Parts

Introduction and Scope

This customer service note provides information to enable customers to easily integrate both leading-edge and legacy Micron® ball grid array (BGA) packages into their manufacturing processes. It is intended as a set of high-level guidelines and a reference manual describing typical package-related and manufacturing process-flow practices.

Because the package landscape changes rapidly and information can become outdated very quickly, refer to the latest product specifications. Contact your sales representative for any additional questions not covered within this guide.

JEDEC Terminology

This document uses JEDEC terminology. JEDEC-based BGA devices in the semiconductor industry are identified by two key attributes:

- Maximum package height (profile)
- Ball pitch

For example: TFBGA = 1.2mm package height and less than 1.0mm ball pitch.

Package descriptors F1 through F6 have been added to provide more detailed ball pitch information for devices with a ball pitch of less than 0.8mm. Within the industry, many memory manufacturers continue to use only the "F" descriptor for any ball pitch of 1.0mm or less. (See JEDEC JESD30E for additional information.)

Maximum Package Height Profiles

Table 1: JEDEC Package Profile Codes

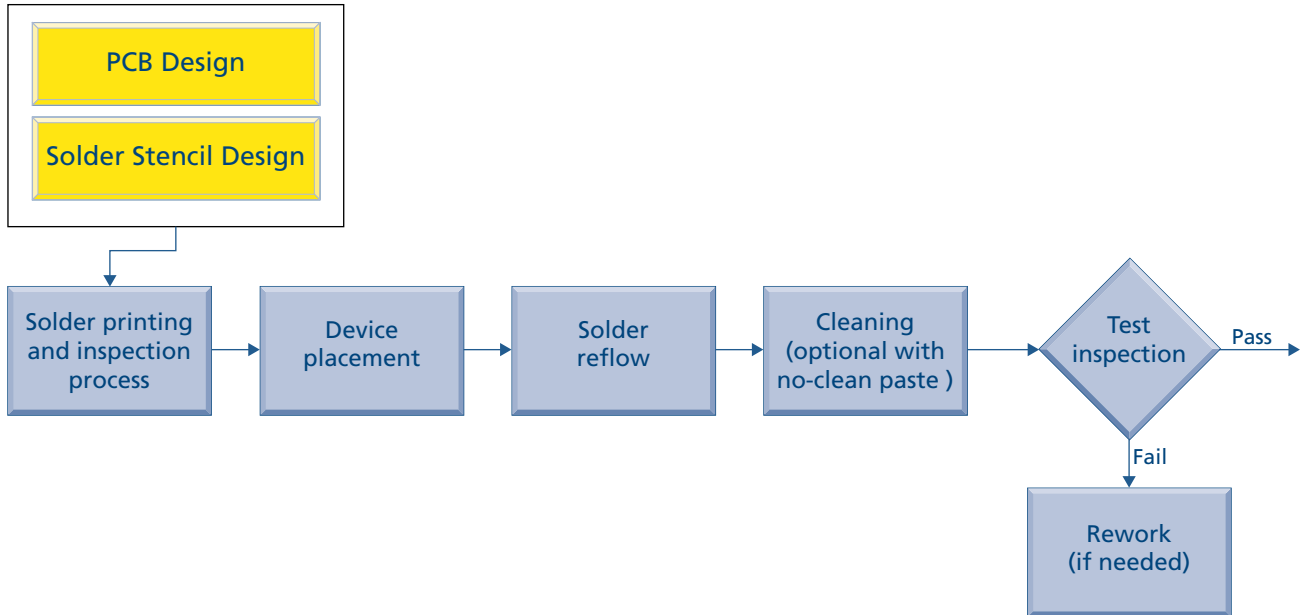
Code	Subcode	Profile Description	Profile Height
-	B2	Extra thick	>3.50mm
-	B1	Very thick	>2.45mm and ≤3.50mm
B	-	Thick	>2.45mm
Blank	-	Standard	>1.70mm and ≤2.45mm
L	-	Low	>1.20mm and ≤1.70mm
T	-	Thin	>1.00mm and ≤1.20mm
V	-	Very thin	>0.80mm and ≤1.00mm
W	-	Very, very thin	>0.65mm and ≤0.80mm
U	-	Ultra thin	>0.50mm and ≤0.65mm
X	-	Extremely thin	≤0.50mm
-	X1	Extra-thin	>0.40mm and ≤0.50mm
-	X2	Super-thin	>0.30mm and ≤0.40mm
-	X3	Paper-thin	>0.25mm and ≤0.30mm
-	X4	Die-thin	≤0.25mm

Table 2: Ball Pitch

Code	Name	Dimension
E	Enlarged	≥1.50mm
Blank	Standard	≥1.00mm and <1.50mm
F	Fine	<1.00mm
	F1 Fine	= 0.80mm
	F2 Fine	= 0.75mm
	F3 Fine	= 0.65mm
	F4 Fine	= 0.50mm
	F5 Fine	= 0.40mm
	F6 Fine	= 0.30mm

Manufacturing Considerations

Figure 1: BGA/LGA Surface Mount Technology (SMT) Process Flow



Creating a High-Yielding Assembly Process

Table 3: Primary Contributing Factors for High Yields

Attribute	Requirement	Comments
Solder paste quality	Uniform viscosity and texture; free from foreign material.	Solder paste should be used before the expiration date. Proper temperature must be maintained during shipment and storage. Paste must be protected from drying out on the solder stencil.
PCB quality	Clean, flat, plated, or coated solder ball land area.	Attachment surface must be clean and free of solder mask residue.
Placement accuracy	Varies	Tight tolerances are not usually required. BGA packages can self-center themselves as long as a major portion (more than 50%) of the solder ball is in contact with the solder-paste-covered land area on the board. Alignment marks (fiducial marks) on the PCB are helpful for verifying correct placement of parts.
Solder reflow profile	Varies	The solder reflow profile is dependent on PCB design, PCB thickness, type of components, component density, and the recommended profile of the solder paste being used. A reflow profile must be developed for each PCB type using various BGA packages (see Figure 3 on page 6). Most solder paste manufacturers provide a suggested thermal profile for their products. These should be reviewed prior to use.

Package-to-Board Assembly Materials and Process

Solder Paste

The quality of the paste print is an important factor in producing high-yield assemblies. Micron has experienced good surface mount results using solder paste with the characteristics shown below.

Table 4: Solder Paste Characteristics

Characteristics	Details
Low residue, no-clean solder paste	Flux class ROL 0 per J-STD-004, alloy SAC 305
Typical particle size	Type 3 (-325 to +500 mesh)
For lead-free BGA applications	Micron has had good results using a solder alloy combination of Sn/Ag/Cu

Solder Stencils

Solder stencil characteristics to consider include:

- Stencil thickness and the etched pattern geometry determine the precise volume of solder paste deposited onto the device land pattern.
- Stencil alignment accuracy and consistent solder volume transfer are critical for uniform reflow-solder processing.
- For BGA applications, a stencil with round apertures or square holes with 5° tapered, trapezoidal openings is recommended.

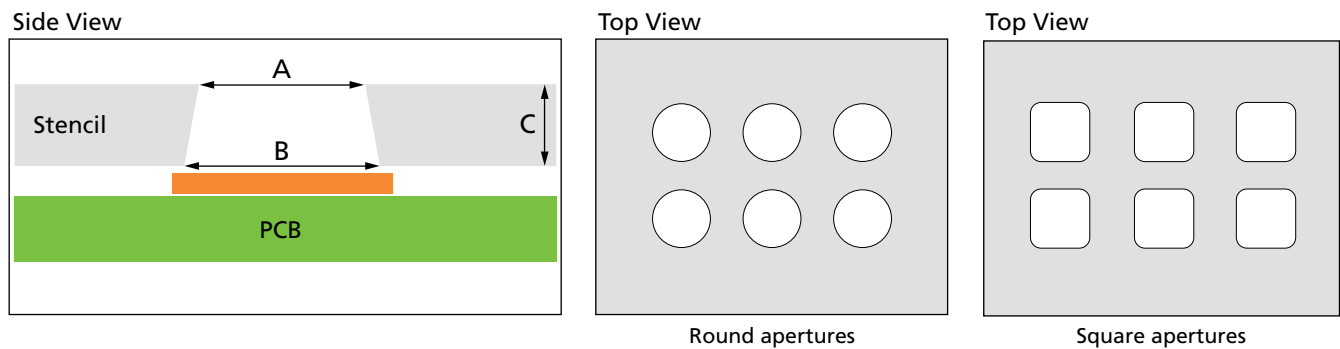
Solder Stencil Guidelines

Table 5: Solder Stencil Dimensions
All dimensions are in millimeters

Feature ¹	0.5mm BGA	0.65mm BGA	0.75mm BGA	0.8mm BGA	1.0mm BGA
Top-of-stencil aperture (A)	0.279	0.33	0.33	0.33	0.33
Bottom-of-stencil aperture (B)	0.30	0.356	0.356	0.356	0.356
Stencil thickness (C)	0.102	0.127	0.127	0.127	0.127

Notes: 1. Letters A, B, and C refer to the dimension indicators in the figure below.

Figure 2: Solder Stencil Aperture Details



To achieve good BGA print characteristics, maintain a diameter-to-stencil thickness ratio of at least 3:1 (larger openings provide better print quality).

Use an opening at least as large as the mounting pad to provide a wide placement window.

Reflow Soldering Parameters: Sn/Pb and Lead-Free

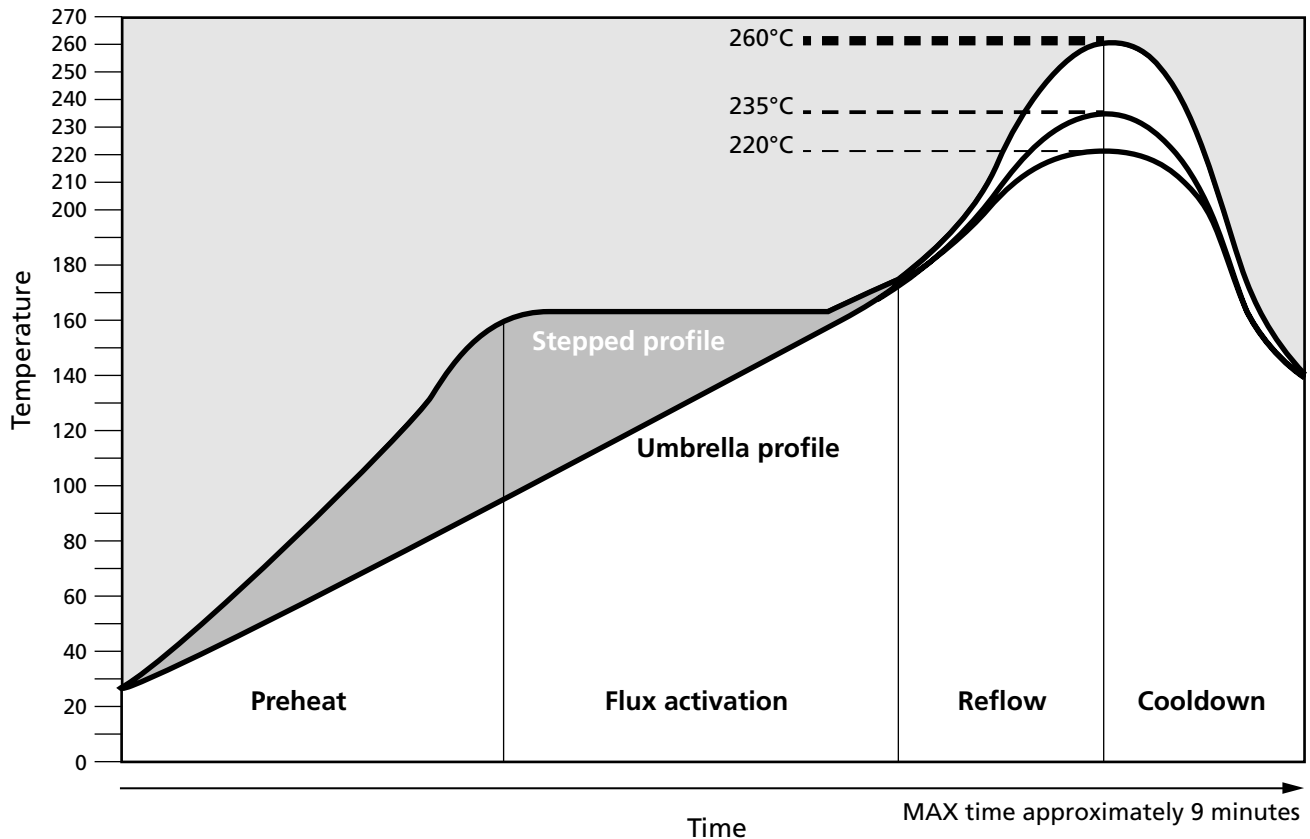
Table 6 and Figure 3 are from Micron Technical Note TN-00-15, "Recommended Soldering Parameters," which defines parameters for reflow profiles using lead solder or lead-free solder. For further details, refer to TN-00-15.

Table 6: Soldering Requirements

	Max Peak Temperature	Max Dwell Time at Peak	Max Heating Rate	Max Cooling Rate	Total Time in Chamber	Number of Reflow Cycles	Notes
Sn/Pb soldering	235°	30s	3°C/s	6°C/s	≈ 9 min.	3	1, 2
Lead-free	260°	30s	3°C/s	6°C/s	≈ 9 min.	3	3

- Notes:
1. For standard Sn/Pb alloys: 63% Sn, 37% Pb; 60% Sn, 40% Pb; and 62% Sn, 36% Pb, 2% Ag.
 2. Some legacy CMOS imaging products are limited to 220°C MAX peak temperature for convection-reflow soldering and wave soldering. If a component is limited to 220°C MAX peak temperature, the floor-life recommendation will be listed on the packaging label. Contact your local Micron sales representative for additional information.
 3. Some lead-free CMOS imaging products are limited to 235°C MAX peak temperature for convection-reflow soldering. If a component is compatible with lead-free processing temperatures, the floor-life recommendation will be listed on the packaging. Contact your local Micron sales representative for additional information.

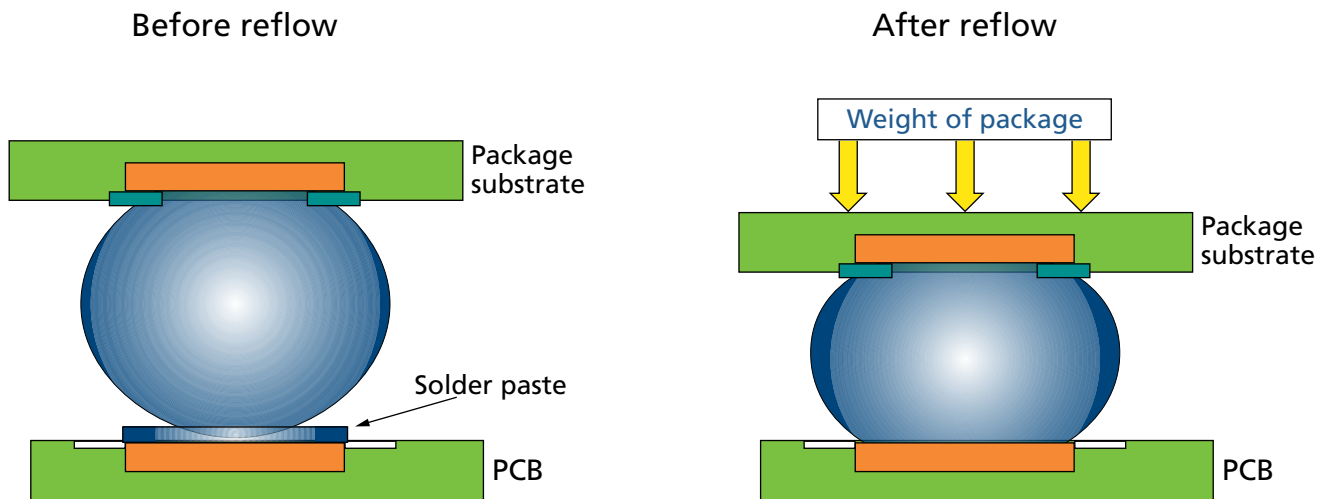
Figure 3: Reflow Profiles



Solder Ball Collapse Behavior for BGA Packages

Coplanarity issues are less critical in BGA packages than in traditional lead-frame packages due to BGA solder ball interconnect collapse at reflow. The maximum coplanarity for BGA devices is typically 0.1mm or less.

Figure 4: Ball Attributes Before and After Reflow



MCP Coplanarity and Warpage Measurement Guidelines

Micron multichip packages (MCPs) meet the coplanarity specifications documented in the package outline drawings provided in Micron component data sheets, as follows:

- 100µm for 1.0/0.80/0.65mm ball pitch packages (0.35–0.40mm ball diameter)
- 80µm for 0.50mm ball pitch packages (0.3, 0.25, and 0.20mm ball diameter)
- This meets the standards described in JEDEC Design Guide 4.5
- Coplanarity measurements are made on production monitor units at room temperature

Warpage across temperature is used when coplanarity is defined by the customer as insufficient to assess the risk-to-SMT yield.

- The Micron warpage target is less than $\pm 100\mu\text{m}$ from flux activation to reflow peak temperatures
- This meets the standards described in Table 1, page 3 of the JEDEC SPP-024A specification

Rework Information

Many manufacturers use a single rework station to incorporate multiple rework process steps, such as component removal, site redress, solder paste/flux application, alignment, component placement and reflow. Characterizing and storing individual component reflow profiles and the advancement of beam-splitting imaging for alignment/placement have simplified the rework process significantly.

One area of concern with rework is thermal separation of adjoining components during the rework process. Some manufacturers have addressed this by designing hot gas nozzles that maintain the keep-out zone around the rework component to thermally isolate adjacent components during the reflow process. Other solutions include temporary heat barriers.

Original equipment manufacturer (OEM) requirements differ when it comes to solder paste and flux-only applications during the rework process. For those requiring solder paste, microstencils and microsqueegees have been developed to correspond with multiple BGA sizes and ball array footprints. These microstencils are aligned using the same beam-splitting imaging as component placement. Microsqueegees enable a simple, uniform solder paste coverage across the microstencil.

- Notes:**
1. Prior to rework, parts must be free from moisture (as per supplier labels)
 2. Under-board preheating is required
 3. Same profile for removal and replacement (maximum three reflows per part recommended)

Flux-Only Attachment

While the use of flux-only attachment has been a common practice for BGA packages in component rework, solder paste is recommended for the best BGA package attachment results.

Before implementing flux-only attachment, however, it is important to note that because flux-only attachment reduces the amount of solder within the solder joint, BGA stand-off is reduced and solder joint reliability may be compromised.

Manufacturers must evaluate flux-only versus solder paste to determine the most suitable process for their specific application.

Reballing

Reballing BGAs is not recommended for production applications. This is primarily due to the various techniques used to remove excess solder (redressing) from the bottom side of the BGA following removal from the PCB. Excessive heat during the redress process can damage the BGA. However, when properly controlled, reballing can be executed successfully. Special reball fixtures and tools are available to simplify and help control this process.

PCB Information

PCB Cleaning

With the elimination of materials containing CFCs, most companies are moving to no-clean or aqueous flux-based systems. Characteristics of these systems include:

- When a low-residue, no-clean solder paste is used, PCB cleaning is generally not required.
- The term “no-clean” describing flux or solder means that there are no harmful residues left on the board to cause corrosion or damage to the components.
- Flux or solder residue from more traditional materials has been shown to be a collection point for outside contamination on the board surface.
- Because so many different types of no-clean solder paste are available, application-specific evaluations should be performed to determine whether any remaining residue must be removed from the boards in final application.
- Evaluations are particularly important if no-clean fluxes are used during rework or manual soldering operations, because nonactivated flux can remain and contribute to corrosion.

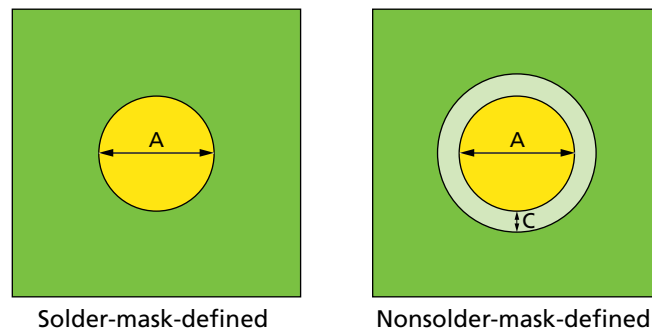
PCB Design Guidelines

PCB design guidelines vary depending on ball pitch, ball diameter, and PCB metal land pad type, including solder-mask defined (SMD) and nonsolder-mask defined (NSMD).

SMD has a solder mask that partially overlaps the metal land pad to determine the metal land pad diameter.

NSMD (also called metal defined) has a solder mask clearance area some distance away from the metal land pad so that the metal land pad diameter is defined by the edges of the metal land pad.

Figure 5: Land Pad Layouts



Notes: 1. A represents the metal land pad diameter; C represents the space between the edge of the metal land pad and the solder mask opening.

Micron recommends that PCB land pad designs maintain a 1:1.2 to 1:1 ratio size between the PCB land pad opening and the package land pad/solder mask opening (SMO) sizes.

Micron BGA and FBGA package ball pitches are typically one of the following dimensions:

- 0.50mm
- 0.65mm
- 0.75mm
- 0.80mm
- 1.00mm

Refer to IPC Publication 7351 (PCB Design Guidelines) for additional details regarding metal land pad dimensions and other PCB design considerations.

References

1. JESD30-B Descriptive Designation System for Semiconductor-Device Packages
2. JEDEC/IPC J-STD-020D.01
3. JESD22-B108A, "Coplanarity Test for Surface-Mount Semiconductor Devices"
4. J-STD-033B.1, Joint IPC/JEDEC Standard for Handling, Packing, Shipping, and use of Moisture/Reflow Sensitive Surface-Mount Devices
5. J-STD-020D.01, Joint IPC/JEDEC Standard for Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Devices
6. IPC - 7526 Stencil and Misprinted Board Handbook
7. IPC - 7525A Stencil Design Guideline
8. IPC - 7351 PCB Design Guidelines

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Revision History

Rev. A	7/11
• Initial release	